AP-523

APPLICATION NOTE

Pentium® Pro Processor Power Distribution Guidelines

November 1995

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1.0. INTRODUCTION

As computer performance demands increase, new, higher speed logic with increased density is developed to fulfill these needs. To reduce their overall power dissipation, modern microprocessors are being designed with lower voltage implementations. This in turn requires power supplies to provide lower voltages with higher current capability. Because of this, processor power is now becoming a significant portion of the system design, and demands special attention. Power distribution requires careful design practices now more than ever. The Pentium® Pro processor has unique requirements for the voltages supplied to it, as well as a new bus implementation, called GTL+, which requires a voltage supply of its own.

For most personal computer designs, a power plane with a mix of high frequency and bulk decoupling capacitors spread evenly across the system board is a low cost way to ensure sufficient power distribution. As the current differences between the low power state and the high power state increase, the cost of the power distribution system becomes significant enough to merit careful calculation. Centralized distribution of power, for example, may no longer be the most cost effective solution to power distribution.

Another side effect of lowering voltages of some components is the existence of multiple voltages within the system. On a basic Pentium Pro processor-based system board there will be 1.5V for GTL+ termination, 2.5V-3.5V for the processor, 3.3V for the chipset and the L2 cache, and 5V for other components. The possibility that any of these voltages may come up before another must be taken into account. This is discussed in Section 3.3.

The reader should be familiar with basic electrical engineering theory, as the first sections of this document will explain in detail the issues involved in designing a system with proper power distribution. The last sections will offer specific solutions for a system containing any number of Pentium Pro processors. This includes a specification for a DC-to-DC converter module.

1.1. Terminology

"Power-Good" or "PWRGOOD" is an active high signal in the system which indicates that all of the supplies and clocks within the system have become stable. PWRGOOD should go active some constant time after 5V, 3.3V and $V_{CC}P$ are stable and should go inactive any time any of these voltages fail their specifications. The time constant should be set such that, in a working system, all clocks and other supply levels have reached a stable condition before PWRGOOD goes active.

"$V_{CC}P$" is the processor core's V_{CC}. "$V_{CC}S$" is always 3.3V.

"GTL+" is the technology used for the bus between the Pentium Pro processor and its chipset. The GTL+ bus and the processor bus are therefore synonymous.

1.2. References

The *Pentium® Pro Processor Developer's Manual, Volume 1: Specifications* (Order Number 242690) is referenced throughout this document.

2.0. TYPICAL POWER DISTRIBUTION

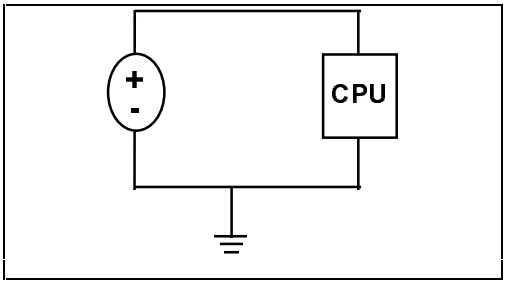

Figure 1. Ideal CPU Power Supply Scheme

Power distribution is generally thought of as *getting power to the parts that need it*. Most digital designers typically begin by assuming that an ideal supply will be provided, and plan their schematics with little thought to power distribution until the end. The printed circuit board designers attempt to create the ideal supply with two power planes in the PCB or by using large width traces to distribute power. High frequency noise created when logic gates switch is controlled with high frequency ceramic capacitors, which are in turn recharged from bulk capacitors (such as tantalum capacitors). Various *rule of thumb* methods exist for determining the amount of each type of capacitance that is required. For Pentium Pro processor designs the system designer will need to reach beyond the rule of thumb and architect the power distribution system with the specifications of the Pentium Pro processor in mind.

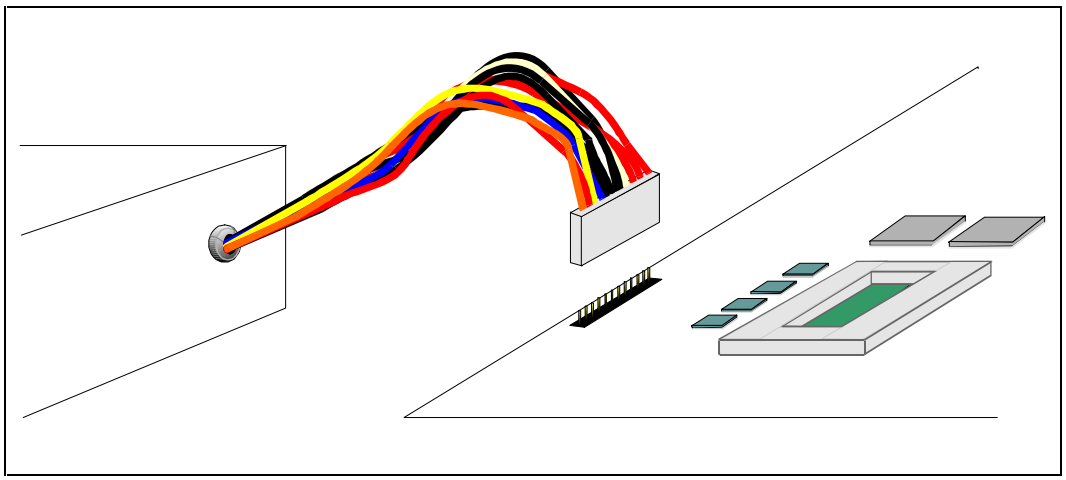

Figure 2. Physical Power Distribution

Figure 1 shows the ideal power model. However, in real systems, the power distribution scheme typically appears as in Figure 2. This system has physical components such as cables, connectors, the PCB, and the component packages.

To completely model this system, one must include the inductance and resistance which exists in the cables, connectors, PCB, and the pins and body of components such as sockets and capacitors. A more detailed model showing these effects is shown in Figure 3. In the past, voltage drops due to inductance (V = Ldi/dt) and resistance (V = IR) have been nearly negligible relative to the tolerance of components in most systems. This has caused the creation of simple rules for decoupling. For example, with the current at 1 Amp, and the tolerance at 250 mV (5% of 5V), one could easily ignore the effects of 25 mΩ of resistance in the distribution path. However, at 10 Amps, this IR drop is equal to the 250 mV tolerance. Similarly, 250 pH of inductance can typically be ignored in a power distribution system, unless current transients of 1 Amp/ns exist, as they do when using the Pentium Pro processor. The Ldi/dt drop in this case is also equal to 250 mV.

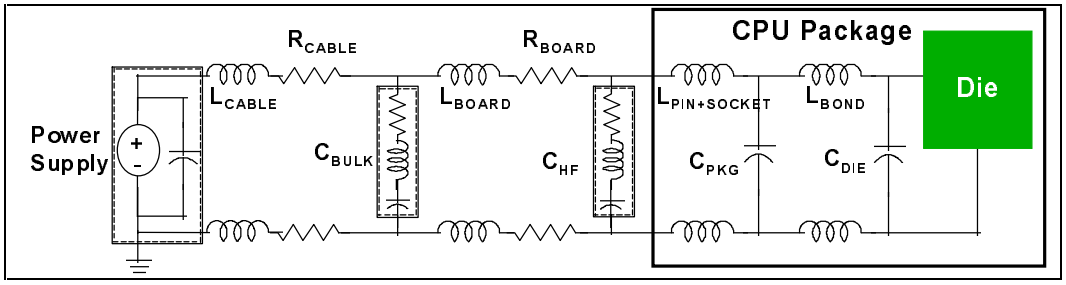

Figure 3. A Detailed Power Distribution Model

The high value of the Pentium Pro processor current and the high rate of change of the current must both be taken into account for a successful design. The requirements of the Pentium Pro processor are described in Section 3, and meeting these requirements is discussed step by step in Section 4.

3.0. PENTIUM® PRO PROCESSOR POWER REQUIREMENTS

This section describes the issues related to supplying power to a Pentium Pro processor using approximate

values. However, actual specifications are documented in the *Pentium Pro® Processor Developer's Manual, Volume 1*.

The Pentium Pro processor with 256-Kbyte cache operates at 3.1V, compared with 3.3V for a Pentium® 815/100 processor, and 5V for previous Intel processors. The tolerance requirement remains at 5%, while the average current demand is approximately 3 times that of the Pentium 815/100 processor. In addition, the Pentium Pro processor shuts off unused units to conserve power, and includes features such as *Stop Clock* and *Auto Halt*, which create load-change transients as high as 8.5 Amps in just one or two bus clock cycles. In this document, a load-change transient is a change from one current requirement (averaged over many clocks) to another. Figure 4 illustrates the V_{CC} and V_{SS} currents of a processor coming out of a low power state and then running in a full power state. The averaged V_{CC} is shown to illustrate what is meant by the term *load-change transient*. V_{SS} current is higher than V_{CC} current in Figure 4 due to power being delivered from the GTL+ bus power supply through the Pentium Pro processor GTL+ buffers. Other transients which must be understood are the switching transients which occur at the processor clock rate, also shown in Figure 4.

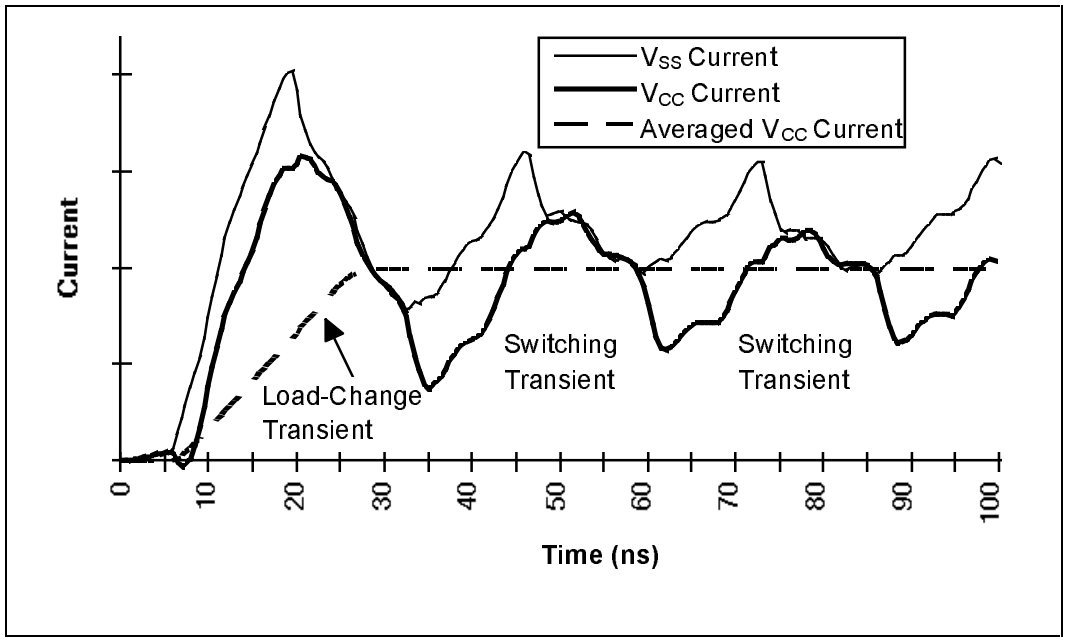

Figure 4. Transient Types

Future Pentium Pro family processors may have a requirement for a separate 3.3V supply for the L2 cache die, as well as higher current requirements, and different voltages for the CPU die.

The GTL+ bus is terminated at each end to a voltage source called V_{TT}. V_{TT} is nominally 1.5V, with a tolerance of 150 mV. This bus implementation allows up to 8 loads, and may be run at speeds up to 66 MHz. Just as the processor can start and stop executing within a few clock cycles, the bus usage will follow.

Each of these concepts is discussed in the following sections. The GTL+ power requirements are discussed in Section 5 and Section 6.

3.1. Voltage Tolerance

The processor voltage tolerance specification has remained at 5%, while the voltage specification has decreased. This causes the absolute tolerance requirement to decrease. For example, 5% of 5V is ±250 mV while 5% of 3.1V is ±155 mV. It is important to note

that this tolerance specification covers all voltage anomalies, including power supply ripple, power supply tolerance, current transient response, and noise. Failure to meet this specification on the low end will result in transistors slowing down and not meeting timing specifications. Not meeting the specification on the high end can induce *electro-migration,* causing damage or reducing the life of the processor.

3.2. Multiple Voltages

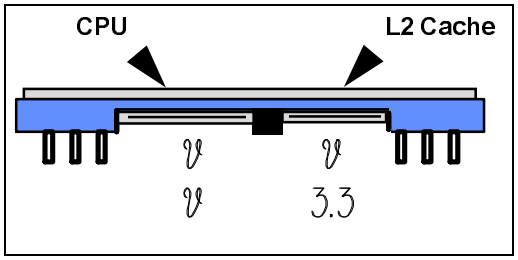

Figure 5. Multiple Voltage Die

While the Pentium Pro processor with a 256-Kbyte L2 cache runs at 3.1V (V), it consists of two separate die. The processor core and the 256-Kbyte L2 cache die are each designed for 3.1V, but future cache die may be designed to run at 3.3V. Also, future Pentium Pro processor components will run at a different voltage than 3.1V. Figure 5 shows a Pentium Pro processor package with the two types of voltage combinations shown beneath it. The Pentium Pro processor definition specifies that *every* L2 will run on either the same supply voltage as the processor core (which may change in the future) or at 3.3V. See the flexible motherboard guidelines in the *Pentium® Pro Processor Developer's Manual, Volume 1* for details.

The Pentium Pro processor package is designed to support future cache die by adding separate 3.3V *cache support* pins to the package. These pins are called $V_{CC}S$ pins, while the primary voltage is supplied on the $V_{CC}P$ pins. See Figure 6 for the location of these pins. For a system to operate seamlessly with a Pentium Pro processor with a 512-Kbyte L2 cache, the $V_{CC}S$ pins simply need to be connected to a well decoupled 3.3V supply. The cache die of each component is bonded internally to receive power either from the cache support pins, or from the main power source as required by the device. Future cache die on $V_{CC}S$ are not expected to exceed a maximum average current (over many cycles) of 2.4A. Note that in components in which the L2 is receiving current from the $V_{CC}S$ pins, the $V_{CC}P$ current will be decreased. The maximum power of a Pentium Pro processor is specified as the sum of the maximum power of each die, not by the maximum current specification of each voltage source.

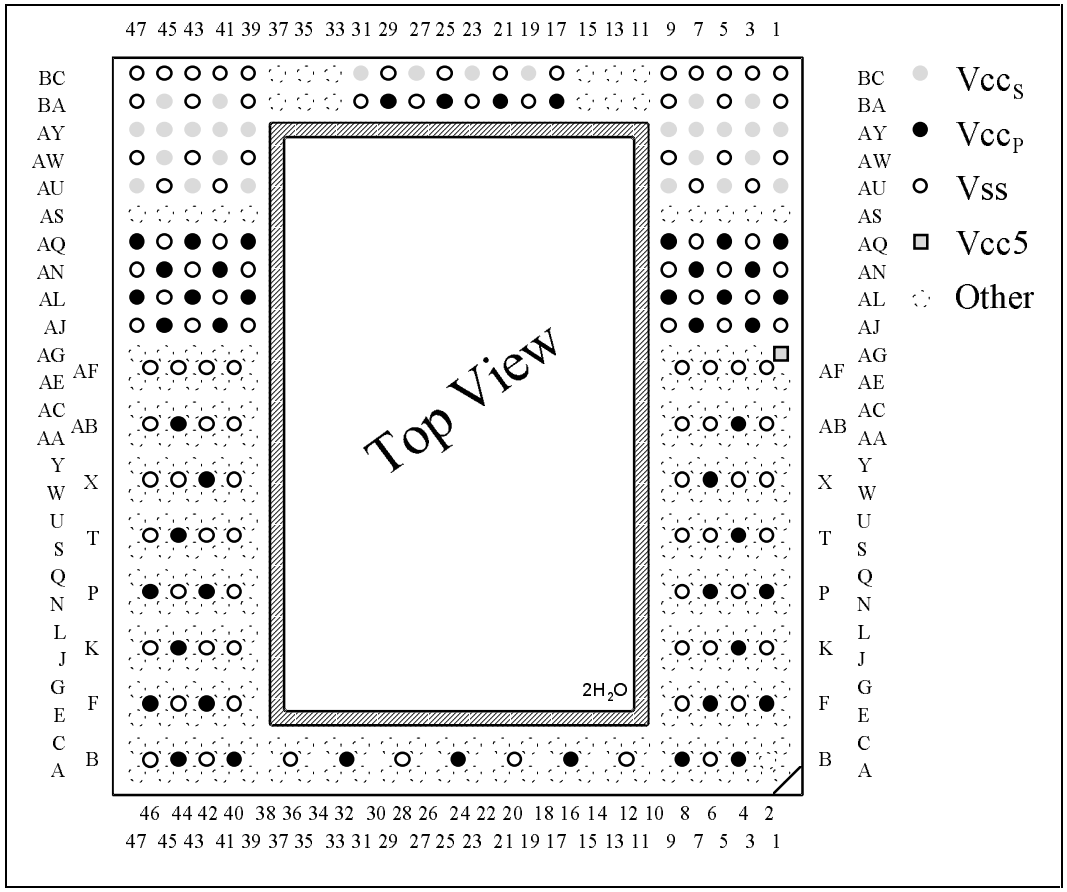

Figure 6. Power Pins of the Pentium® Pro Processor Package - Top View (Through the Package)

A system designer planning for upgrade potential should also be aware that future devices beyond the Pentium Pro processor may require a voltage other than 3.1V. This may range from 2.5V to 3.5V. To support this level of upgrade potential, the power source for the *main* processor supply should be designed with the ability to be easily configured to provide a voltage within the range of 2.4V to 3.5V. Note that the cache will either run at the **same voltage** as the processor, **or** at 3.3V, using the cache support pins. One easy way to support this range is with a replaceable power module. Another is by changing the set point of the regulator via a variable resistor, or by using the processor's Voltage ID pins with a resistor tree or a Digital to Analog converter (DAC). The voltage ID scheme is described fully in the *Pentium® Pro Processor Developer's Manual, Volume 1*. Intel has worked with power supply vendors to create replaceable voltage regulators which support voltage selection. See your local field applications engineer for assistance.

Another voltage is required for the GTL+ bus. This level is called V_{TT}, and is set at 1.5V. This voltage is discussed in Section 5, but is important in the discussion of Voltage Sequencing in Section 3.3 as well.

3.3. Voltage Sequencing

When designing a system with multiple voltages, there is always the issue of ensuring that no damage occurs to the system during *voltage sequencing.* Voltage sequencing is the timing relationship between two or more voltages, such as 3.3V and $V_{CC}P$. Sequencing applies when the power supply is turned on or off, or enters a failure

condition. Sequencing applies to the power voltage levels and the levels of certain other crucial signals.

Figure 7 shows an example of power voltage sequencing. Here voltage levels A and B are shown to trade places with each other. On power-on, A-B may be larger at any point than they will be once they reach their nominal levels. On power-off, the voltage B input may actually be higher than the voltage A input for some period of time. The Pentium Pro processor, GTL+ bus, and Intel's chipsets have been designed such that no additional circuitry is required in the power system to ensure the order of voltage sequencing. However, systems should be designed such that neither supply stays on permanently while the other is off. The long term reliability of the component can be compromised by excessive exposure to these conditions.

The discussion following is simplified by assuming the worst case which is one voltage on while the other is off. See Figure 8 and Figure 9 for highly simplified models of the buffers that show the ESD protection diodes. This model is provided for discussion purposes only and is not meant to imply any implementation scheme.

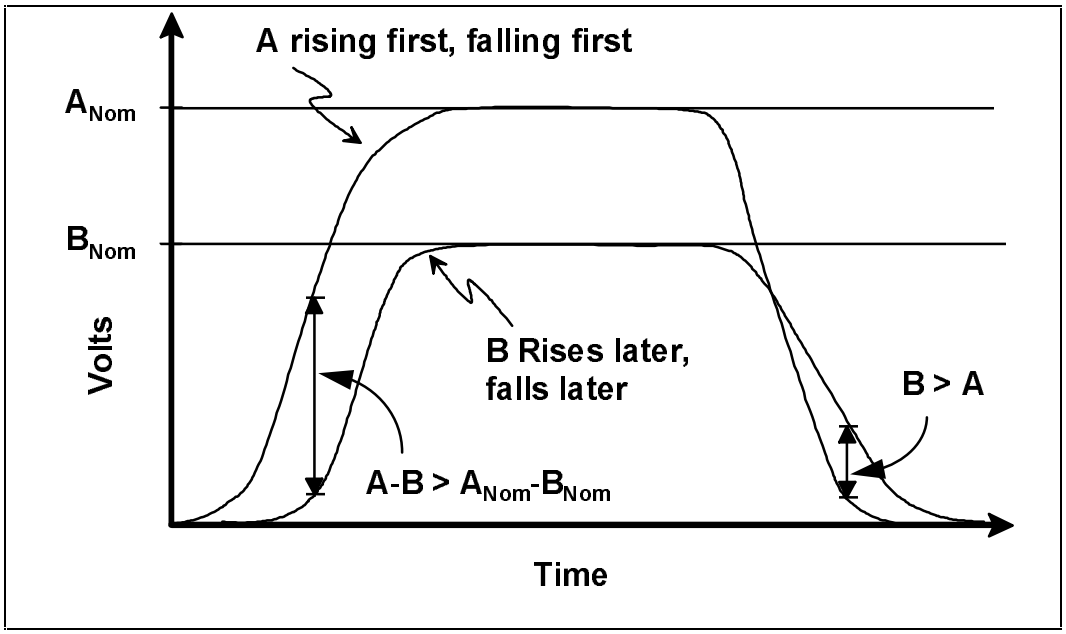

Figure 7. Voltage Sequencing Example

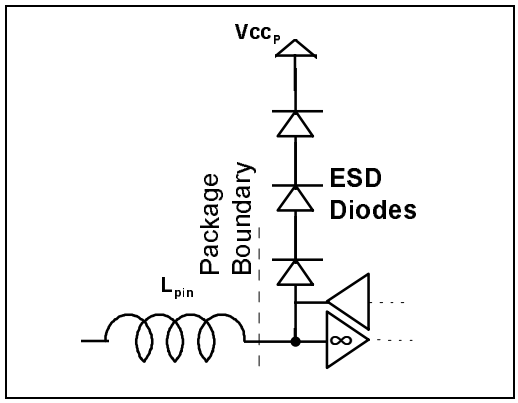

Figure 8. Tolerant ESD Diodes

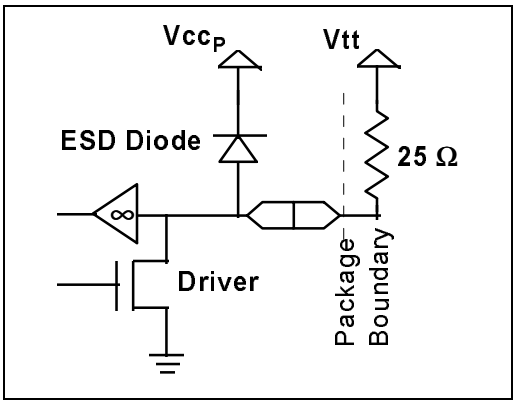

Figure 9. GTL+ ESD Diodes

3.3.1. 3.3V TOLERANT SIGNALS

The 3.3V tolerant buffers are open drain. When the $V_{CC}P$ supply is on, and the 3.3V supply is off, the ESD protection diodes of the buffers are reverse biased and no power is supplied to the signal lines. As the processor sees RESET#, the outputs switch to the high or inactive state so bus contention after 3.3V comes up is avoided.

If the 3.3V supply is on while the $V_{CC}P$ supply is off, the 3.3V supply will deliver current to the Pentium Pro processor core through the string of three ESD protection diodes connecting the pads to V_{CC}. If a pull-up is used for the high level of the signals, then 150 ohms will allow a maximum of only 9 mA of current to be supplied to the core per pad cell. If the inputs are driven by a CMOS output, then the current from the output should be limited to 200 mA maximum output current per Pentium Pro processor pin.

If $V_{CC}P$ is used as the high level for the 3.3V tolerant signals, then no sequencing issue exists.

3.3.2. GTL+ SIGNALS

The GTL+ outputs are also open drain. When the $V_{CC}P$ supply is on and V_{TT} is off, all inputs appear low and there will be no current flowing on the GTL+ bus.

If V_{TT} is on and $V_{CC}P$ is off, the GTL+ bus will attempt to power up the core through the ESD protection diode. The resulting V_{CC} level will be low enough that no significant current will be consumed by the core.

NOTE

Every device on the bus must have power in order for the GTL+ bus to operate properly.

3.3.3. MEMORY SIDE SIGNALS

The 5V tolerant signals are internally buffered in a similar manner. When using 3.3V DRAM there are no memory side sequencing issues. When the 5V supply is on to 5V DRAM and the 3.3V memory controller supply is off, the CAS lines may be floating. This could cause the DRAM to drive 5V signals to a component that has no voltage applied. The system should provide weak pull-ups to 5V on the CAS lines to prevent the 5V DRAM devices from driving 3.3V inputs when there is no power to the memory controller.

By providing the memory controller with the PWRGOOD signal (as described in Section 1.1), it will drive the CAS lines of the DRAM inactive, and reset the data buffers as soon as it receives 3.3V. This will hold the DRAM outputs off and keep the chipset buffer components in reset during a period of power supply stabilization. This includes a poor V_{TT} that would prevent the GTL+ bus RESET# signal from being created correctly. This action protects these devices from producing bus contention between themselves.

3.3.4. PCI SIDE SIGNALS

PCI_RST# tells all PCI devices to remain in a tri-state condition. This signal will be held active by the PCI bus controller when it is receiving power and its PWR_GD signal is inactive. The PCI bus controller will also tri-state its signals during this time. In addition, the PCI

inputs use a 5V input for their ESD protection. This eliminates any issue with turning on its ESD diodes.

If there are 5V PCI cards in the system, it would also be prudent to supply a weak pull-down on the PCI_RST# line for the event that 5V is on while 3.3V is off.

3.3.5. CLOCK INPUT

The clock input frequency must never exceed the intended final value while the PWRGOOD signal to the processor is active. (See terminology in Section 1.1)

PWRGOOD should be inactive anytime that $V_{CC}P$ or 3.3V are invalid. This can be accomplished by logically OR-ing the PWRGOOD signals from both supplies, and connecting this output to the chipset and the Pentium Pro processor Power-Good inputs (pin names may vary) for reset generation. (In this case, PWRGOOD is a signal from each supply that signals when its voltage level is stable and within tolerance.)

3.3.6. CLOCK RATIO INPUTS

The pins A20M#, IGNNE#, LINT1, and LINT0 are shared with the function for programming the PLL core clock multiplier ratio. These pins control the setting of the clock multiplier ratio during RESET# and until two clocks beyond the end of the RESET# pulse. At all other times their functionality is defined as the compatibility signals that the pins are named after. These signals have been made 3.3V tolerant so that they may be driven by existing logic devices. This is important for both functions of the pins.

Figure 10 shows the timing relationship required for the clock ratio signals with respect to RESET# and BCLK. Table 1 shows the timing parameters. Note that the minimum setup time for these signals is 1 ms. This table also shows the timing relationship of the compatibility signals. A signal called CRESET# (CMOS Reset) is shown, with the timing needed for controlling the multiplexing function required to share the pins. This may be provided by the chipset.

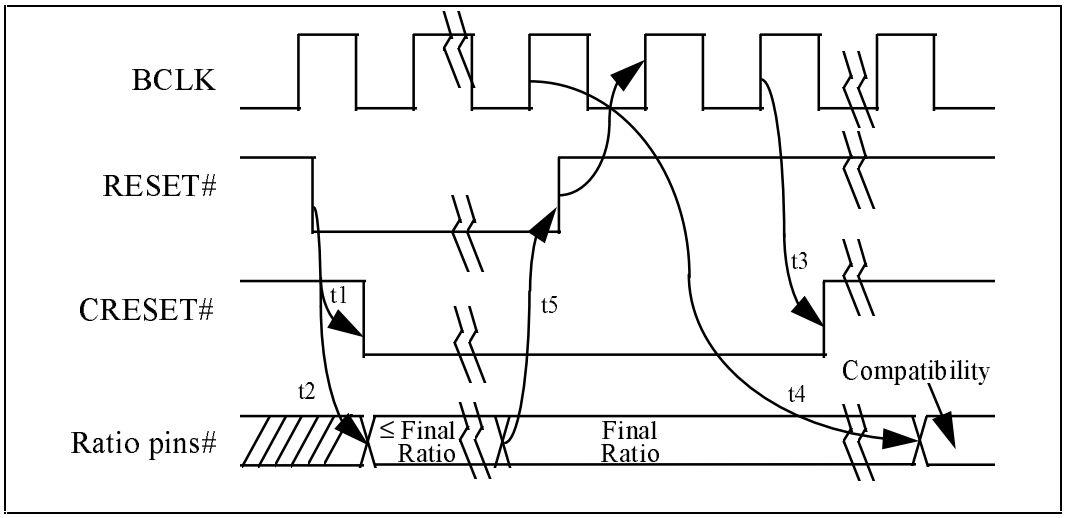

Figure 10. Timing Diagram of Compatibility Pins

Table 1. Timing Parameters of Compatibility Pins

t#	Parameter	Minimum	Maximum	Units
t1	RESET# active to CRESET#		10	ns
t2	RESET# active to Ratio Delay		5	BCLKs
t3	BCLK to CRESET# Inactive		10	ns
t4	BCLK to Compatibility		20	BCLKs
t5	Ratio Setup to RESET# rising	1		ms

Using CRESET#, the circuit in Figure 11 can be used to share the pins. The pins of the processors are bussed together to allow any one of them to be the compatibility processor. The component used as the multiplexer must not be powered by more than 3.3V in order to meet the 3.3V tolerant buffer specifications of the Pentium Pro processor. The multiplexer output current should be limited to 200 mA maximum, in case the 3.1V supply does not come up.

The pull-down resistors between the multiplexer and the processor (1K ohms) forces a ratio of 2:1 into the processor in the event that the Pentium Pro processor powers up before the multiplexer and/or the chipset. This prevents the processor from ever seeing a ratio higher than the final ratio. These are unnecessary if another known ground path through the multiplexer exists when 3.3V is off.

If the multiplexer were powered by $V_{CC}P$, CRESET# would still be unknown until the 3.3V supply came up to power the chipset. A pull-down can be used on CRESET# instead of the four between the multiplexer and the Pentium Pro processor in this case. In this case, the multiplexer must be designed such that the compatibility inputs are truly ignored as their state is unknown.

In any case, the compatibility inputs to the multiplexer must meet the input specifications of the multiplexer. This may require a level translation before the multiplexer inputs unless the inputs and the signals driving them are already compatible.

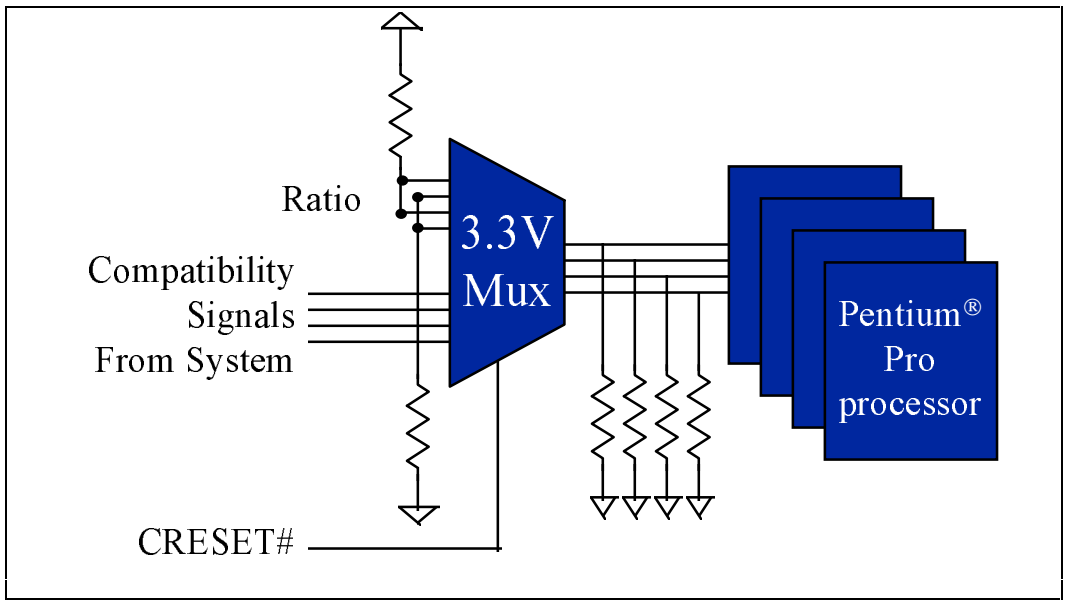

Figure 11. Schematic of Pin Sharing

3.3.6.1. Mixed Frequency Processors

In order to support different frequency multipliers to each processor, the design will require four multiplexers. Before implementing this strategy, one should understand how useful this will be to the operating systems running on the system.

3.3.6.2. FRC Mode

For FRC mode processors, one multiplexer will be needed per FRC pair, but the multiplexer will need to be able to be clocked using BCLK and meet setup and hold times to the processors. This may require the use of high speed programmable logic.

4.0. MEETING THE PENTIUM® PRO PROCESSOR POWER REQUIREMENTS

To solve the needs of the Pentium Pro processor, one must merely be aware of the issues described above and design the system appropriately. This involves making many tradeoffs between power supply, distribution and decoupling technologies. This section discusses how to design a system using the more accurate power distribution model shown in Figure 3, one step at a time.

4.1. Voltage Budgeting

Before beginning the design of a power distribution system one must have an idea of how the tolerance specification will be budgeted to each of the components involved. This will provide a target for each component and helps reduce iterations to reach a solution. The Pentium Pro processor requires that the system meet a 5% tolerance specification. This is equivalent to 155 mV above and below the nominal 3.1V. Do not include voltage drops of the Pentium Pro processor socket, pins etc. since these are taken into account beyond the 5% tolerance specification. This is the budget the system designer has to work with which leaves the model in Figure 12 to work with at the Pentium Pro processor socket pins.

The components that should be included in a voltage budget are shown in Table 2 along with example values for each. There are two budgets shown since different components are more prevalant at different times. Inductive effects are significant early in a current transition while di/dt is high and are shown in the high frequency (HF) budget. Capacitive effects are more important once the HF capacitors have released their charge and are shown in the low frequency (LF) budget. Board resistance losses must always be included, while ESR losses only need to be included for capacitors while they are delivering current. Capacitor ESR is shown as a loss in both budgets.

This may make a good starting point for any system budget, but will be adjusted to suit that system's needs. Each component is discussed in the following sections.

Table 2 assumes that voltage drops break down over time in a discrete manner. Ultimately the power distribution should be simulated by the designer which will allow the budget to be loosened.

Table 2. A Sample Voltage Budget

Component	HF Budget in mV	LF Budget in mV
Tolerance Specification	155	155
Regulator Set Point Tolerance	-25	-25
Inductive losses in HF Capacitors	-60	0
HF Capacitance ESR	-30	0
Bulk Capacitance ESR/ Capactance Sag	0	-60
Inductive Losses in Board	-10	0
Resistive Losses in Board	-10	-10
Ripple, Noise	-10	-10
Margin	10	50

4.2. Supplying Power

The start of a power distribution system is the source of power, or the power supply. The voltage required by the Pentium Pro processor is probably not already available from a standard supply and will need to be created as Pentium Pro processor designs are developed. The new voltage can be generated from an AC input (such as the line voltage) or from another DC supply. Also, the voltage can be created within a central power supply unit and distributed, or created locally to the load. The many tradeoffs involved are discussed here.

In order to maintain power supply tolerance, either local regulation or a power supply with remote sense capabilities is required. This is due to the higher current requirements of the Pentium Pro processor. Typically there is a DC loss over the power distribution system due to the resistance of such things as cables, power planes, and connectors. These are the first two components of the complex model being discussed. They are shown in Figure 12 as R_{BOARD} and R_{CABLE}.

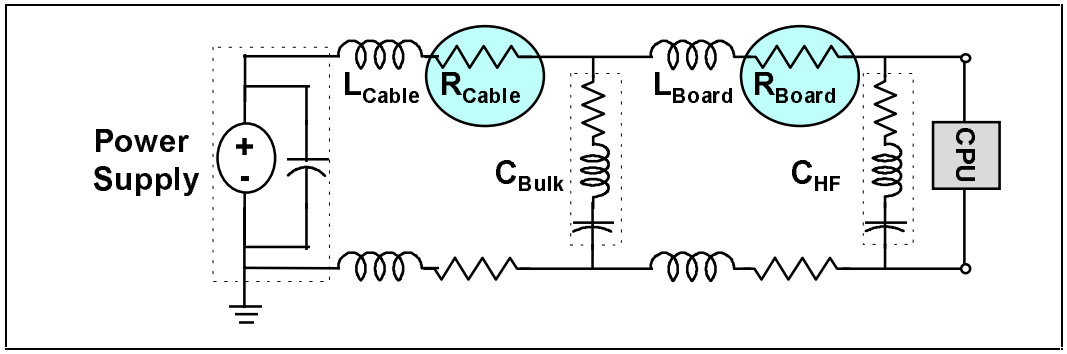

Figure 12. System Design Model

This loss can be represented as $\Delta V = I \times R$, where ΔV is the voltage loss, I is the current and R is the effective resistance of the distribution system. When the average current is continuous, the power supply can be designed to compensate for this loss by setting the voltage slightly higher than the nominal value. This ensures that the voltage at the farthest reaches of the system is still within specification. However, when the current has the ability to change significantly between a high and a low state (i.e. ΔI is high), ΔV changes significantly as well. This change in voltage can be represented as $\Delta V = \Delta I \times R$. This loss can become significant due to the tighter tolerance specification of the Pentium Pro processor requiring that the total ΔV at the CPU socket be within 5% of the nominal voltage.

Local regulation is the use of a supply or regulator near the load to create the voltage needed. One practical example of this is a local DC-to-DC converter. In this application, a higher DC voltage is typically distributed to the area where the load exists and then is converted to a lower level using either a linear or a switching regulator. By distributing a lower current at a higher voltage, the unwanted losses (I x R) are minimized. (This is done in high tension lines to distribute electricity from the generating source to local residential use). More importantly however, the voltage is regulated locally which minimizes DC line losses by eliminating R_{CABLE} and reducing R_{BOARD} on the processor voltage.

If local regulation is not appropriate, then a power supply with remote sense may be used. A power supply typically regulates the voltage at its terminals before cabling to the board. Again, changing distribution losses based on the current demand make it difficult to hold a tight tolerance at the load. A remote sense, shown in Figure 13, solves this problem by running a separate

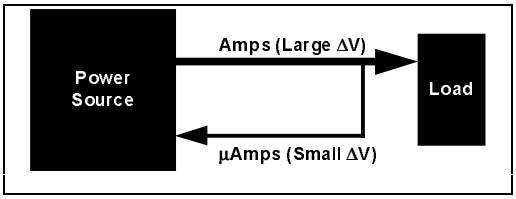

Figure 13. Remote Sense

connection from near the load to the feedback loop of the power supply. This line will have very low current draw

(μAmps) and will not suffer from the line losses described above. This allows the supply to regulate its output based on the voltage level at the load that *is* affected by the line losses. The down-side of this method is the added inductance due to cabling to a power supply and the noise induced in the remote sense feedback signal. Section 4.3 explains why this is an issue. Another difficulty is finding a representative load point that applies for all processors when there is more than one in the system.

In either case the accuracy of this voltage can be maintained fairly easily at ±2%, plus a small ripple and noise budget, under a *stable* load. However, further demands of the Pentium Pro processor will tax this supply. With the large current transients developed by the processor, extreme care must be exercised to eliminate noise coupling and ringing when using remote sense feedback.

4.2.1. LOCAL DC-TO-DC CONVERTERS VS. CENTRALIZED POWER SUPPLY

Most desktop computers today utilize a self-contained multiple output power supply. This is convenient and cost effective as it isolates the issues of power generation from the system designer and allows the creation of a large reusable sub-system. However, lower operating voltages and increased transient response make long bus distribution schemes and self-contained supplies less suitable due to the resistance and inductance of the distribution scheme. The use of distributed local DC-to-DC converters provides another alternative.

Another benefit of distributed local DC-to-DC converters is upgrade potential. They allow for socketed and/or voltage selection and regulation. Sockets allow modules to be added or replaced as required while self adjusting regulators can be set to meet the varying needs of the processor socket.

While the decision lies in the hands of the system designer, Intel recommends the use of local regulators. Converter sockets meeting the upgrade specification in the *Pentium® Pro Processor Developer's Manual, Volume 1* can then be installed by each empty Pentium Pro processor socket to provide an inexpensive upgrade strategy. Utilized Pentium Pro processor locations can be powered by a socketed regulator or one whose output levels can be selected.

4.2.2. AC VS. DC INPUT VOLTAGE

The new Pentium Pro processor DC voltage can be created directly from the line voltage or from a low voltage AC or DC tap of the central power supply.

Creating a DC voltage from an AC voltage is generally *easier* than converting from one DC level to another. This is due to the fact that a DC voltage first needs to be *chopped* in order create an alternating voltage that can be then stepped up or down. Typically however, PC power supplies today do not provide AC voltage taps to the system.

Creating the additional DC voltage from the line voltage requires the addition of an extra winding to the line transformer. This tends to be rather costly, and will suffer more from issues of distribution explained in the next sections. Changing the output voltage in this system requires changing the transformer, which makes the design less versatile.

Creating the additional DC voltage from an existing DC voltage requires a DC-to-DC converter. These converters work well in the PC market as they can be designed to work off the existing 5V or 12V taps of standard PC power supplies, and can be manufactured in high volumes. They can be placed very near the Pentium Pro processor, thus reducing distribution loss issues, or designed into the existing power supply case. They can also be designed to have a selection of output voltages, as well.

4.2.3. LINEAR REGULATORS VS. SWITCHING REGULATORS

A linear regulator is a simple device that drops a variable voltage across itself in order to maintain an output voltage within tolerance regardless of load changes (within its specifications). Due to the simplicity of this device, its reaction time is fairly quick, on the order of 1μS. However, the efficiency of a linear regulator is fairly poor. Its efficiency drops off as the input voltage and output voltage become farther separated as evidenced in Equation 1.

Equation 1 Loss Within a Linear Regulator

$$P_{LOSS} \approx (V_{IN}-V_{OUT}) \times I.$$

The linear regulator also requires a minimum drop from the input to the output of about a diode drop (0.5V-1.0V), making it impossible to have small changes from V_{IN} to V_{OUT}.

Table 3. Efficiency of a Linear Regulator

V_{OUT}	Efficiency with V_{IN} of 5V	Power loss at 9.9 Amps
3.3	66%	16.8W
3.1	62%	18.8W
2.5	50%	24.8W

The efficiency of a linear regulator can be approximated by the formula efficiency = V_{OUT}/V_{IN}. The power loss and efficiency are shown in the Table 3 where V_{IN} has been left at 5V and the current delivered has been fixed at 9.9 Amps. The power loss is fairly significant for a linear regulator.

Although linear regulators tend to have faster reaction times than switching regulators, the power loss in a linear regulator is high enough that the use of a switching regulator should be considered at these higher output current ratings. An 80% efficiency can be achieved using a 3.1V switching regulator at 9.9 Amps.

A switching regulator first *chops* the input voltage to make it *AC-like*. The faster it switches or chops, the faster the reaction time of the converter can be. The faster the reaction time, the less capacitance will be required to support it. Low end switching regulators operate at a 100 kHz switching rate, while high end devices start at 1 MHz.

4.3. Decoupling Technologies and Transient Response

As shown earlier, inductance is also an issue in distribution of power. The inductance of the system due to cables and power planes further slows the power supply's ability to respond quickly to a current transient.

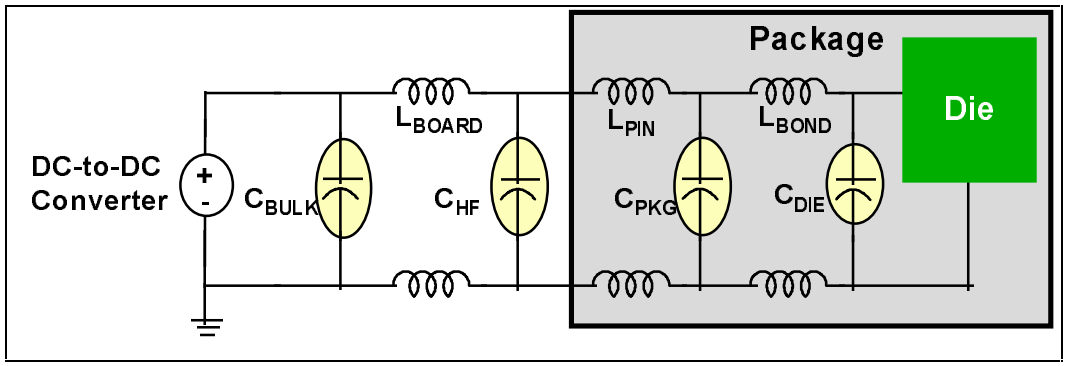

Figure 14. Location of Capacitance in a Power Model with a DC-to-DC Converter

Decoupling a power plane can be broken into several independent parts. Figure 14 shows each of the locations where capacitance could theoretically be applied. The closer to the load the capacitor is placed, the more inductance that is bypassed. By bypassing the inductance of leads, power planes etc., less capacitance is required. However, closer to the load there is less room for capacitance. Therefore tradeoffs must be made.

Typically a digital component will cause switching transients. These are the sharp surges of current that occur at each clock edge and taper off by the end of the cycle as shown in Figure 4. The Pentium Pro processor has been designed such that it manages the highest frequency components of the current transients. This has been accomplished by adding capacitance to the package (C_{PKG}) as well as directly on the die (C_{DIE}). To lower bond wire and pin inductance (L_{BOND} and L_{PIN}) as well as the board inductance (L_{BOARD}), the Pentium Pro processor is designed with approximately 70 ground pins and 45 power pins. (The larger number of ground pins than power pins is to account for the current

requirements of the GTL+ open drain gates). These processor design considerations reduce the current slew rate to the order of 1A/ns at the pins. Outside the package, the 1A/ns current slew rate is supplied current by local high frequency, low inductance decoupling (C_{HF}) such as ceramic capacitors. Larger bulk storage (C_{BULK}), such as electrolytic capacitors, supply current during longer lasting changes in current demand by the component, such as coming out of an idle condition. Similarly, they act as a storage well for current when entering an idle condition from a running condition.

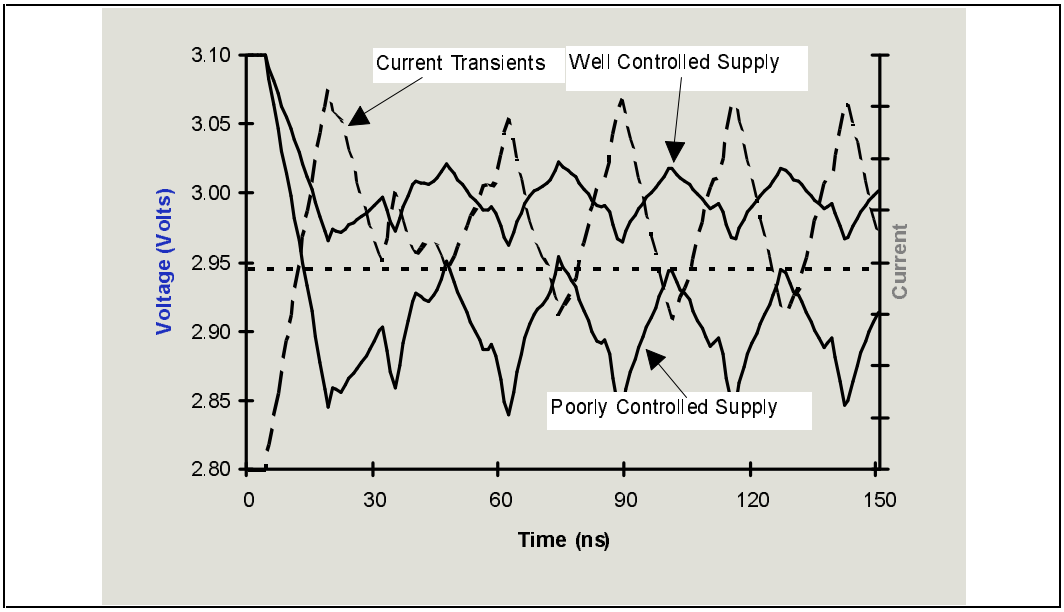

Figure 15. Effect of Transients on a Power Supply

All of this power bypassing is required due to the relatively slow speed at which a power supply or DC-to-DC converter can react. A typical voltage converter has a reaction time on the order of 1-100µs while the processor's current transients are on the order of 1 to 20 ns. Bulk capacitance supplies energy from the time the high frequency decoupling capacitors are drained until the power supply can react to the demand. More correctly, the bulk capacitors in the system slow the transient requirement seen by the power source to a rate that it is able to supply, while the high frequency capacitors slow the transient requirement seen by the bulk capacitors to a rate that they can supply. Figure 15 shows a poorly controlled supply versus a well-controlled supply during an increase in current demand. Notice how the poorly controlled supply dips below the allowed tolerance specification. A similar situation exists as the current demand decreases.

A load-change transient occurs when coming out of or entering a low power mode. For the Pentium Pro processor this load-change transient can be on the order of 9 Amps. These are not only quick changes in current demand, but also long lasting average current requirements. This occurs when the STPCLK# pin is asserted or de-asserted and during *Auto Halt.* Auto Halt is a low power state that the processor enters when the HALT op-code is executed. Note that even during normal operation the current demand can still change by as much as 7 Amps as activity levels change within the Pentium Pro processor component.

To maintain voltage tolerance during these changes in current, both high frequency decoupling capacitors and slower, high-density bulk capacitors with low ESR will be required. These components need to be chosen based on a thorough analysis.

4.3.1. BULK CAPACITANCE

To understand why just adding more capacitance is not always effective, one must consider the Effective Series Resistance (or ESR) of the capacitance being added. This is the inherent resistance of the capacitor plate material. One way to understand where *ESR* comes from, and how to recognize a low ESR capacitor, is to analyze a cylindrical capacitor. By unrolling the metal of the capacitor it appears as a sheet. This sheet has some linear resistance in Ω/inch. A longer sheet (Bigger diameter capacitor) increases ESR. A wider sheet (Taller capacitor) decreases the ESR.

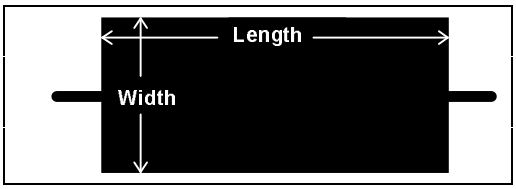

Figure 16. ESR Cylindrical Capacitor

Another effect is the fairly high inductance of the bulk capacitors. These elements can be modeled as shown in Figure 17.

Again, this was taken from the complex model of Figure 3. Overcoming ESR is discussed here while assuming for now that the inductance effect will be addressed by the high frequency decoupling capacitors discussed in Section 4.3.2.

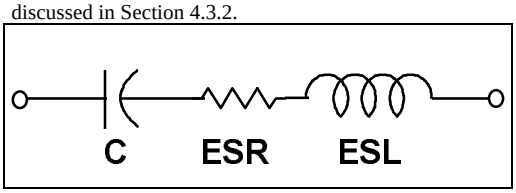

Figure 17. A Capacitor Model

Figure 18 shows the relationship between current delivered (with a 60 mV budget) and the ESR of the capacitors. As can be easily seen, even with infinite capacitance, 6 mΩ of ESR at 10A drops the full budget of 60 mV as shown in Equation 2.

Equation 2. ESR Allowed for 60 mV Budget

$$R = 60mV / I$$

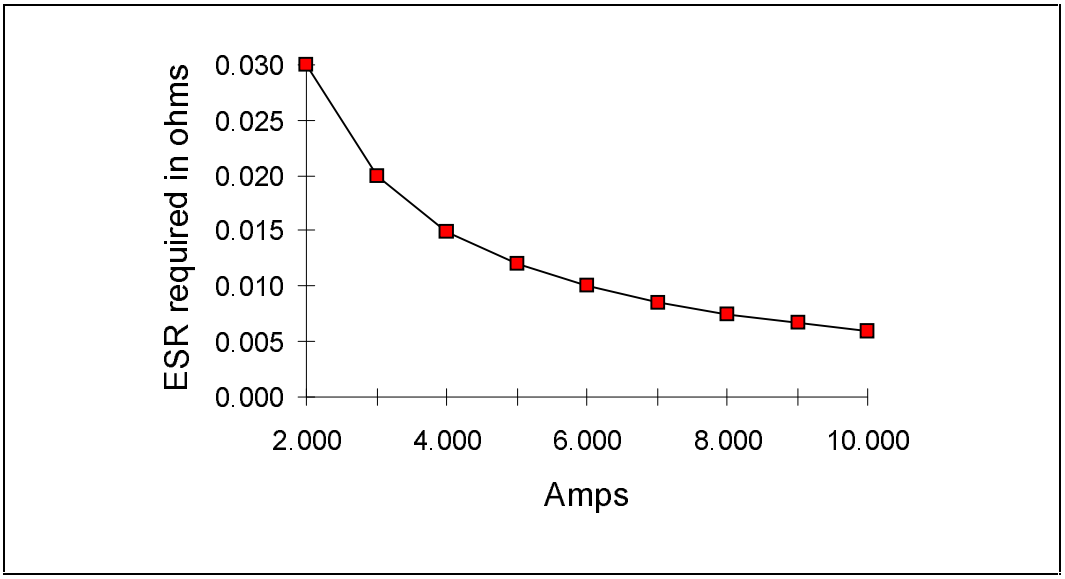

Figure 18. ESR Required for Various Current Demands

Another useful formula for estimating the amount of bulk capacitance required is shown in Equation 3. This ignores the ESR of the component but furnishes the amount of capacitance that would be required from an ideal component.

Equation 3. Capacitance for an Ideal Capacitor

$$C = \frac{\Delta I}{\Delta v / \Delta t}$$

ΔI represents the current that the bulk capacitance must be able to deliver or sink. This is equal to the difference between high and low current states since the power supply will initially continue to supply the same current that it had been prior to the load change. Δv is the allowable voltage change budgeted for bulk capacitive sag (discharge) over the period Δt. Δt is the reaction time of the power source.

Assuming some representative numbers for I, ΔV, and Δt, the capacitance required is shown by Equation 4.

Equation 4. Capacitance needed if ESR is 0 ohms

$$C = \frac{8.5A}{0.060V / 30x10^{-6}\,s} = 4250\mu F$$

Combining the above formulas to remove the resistive drop from the budget for the bulk capacitance gives Equation 5.

Equation 5. Capacitance vs. ESR

$$C = \frac{I \times \Delta t}{\Delta V - I \times ESR}$$

This equation leads to the capacitance vs. ESR graph shown in Figure 19, when ΔV is assumed to be 60 mV, I is assumed to be 8.5A, and the reaction time (Δt) of the power source is 30 µs. The shaded area of the graph covers capacitance types that are insufficient for this application. Again this provides a figure that can be used to get a feel for the type of capacitors required. For example, to satisfy this equation one could use twelve 1000 µF capacitors if the ESR of each was 53 mΩ. The parallel resistance of 12 capacitors would be 4.4 mΩ and the parallel capacitance would be 12,000 µF, which falls in the white zone of the graph in Figure 19.

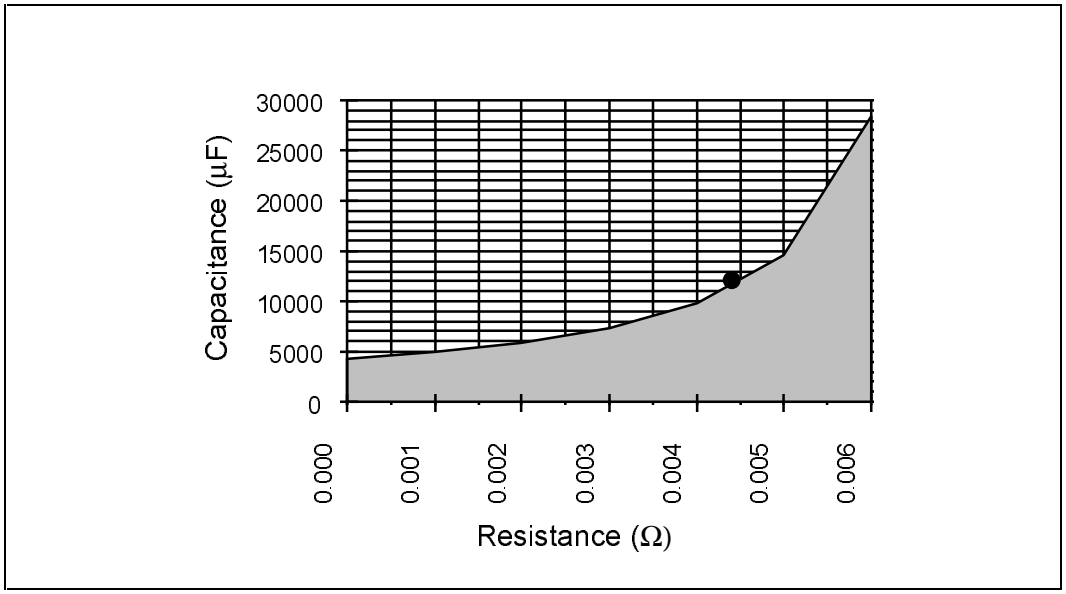

Figure 19. Capacitance Required vs. ESR at 8.5A, 60 mV ΔV and 30µs Δt

This is a fairly conservative analysis. Using a reaction time for a power source assumes that the power source does not compensate at all for the change in current demand until Δt has passed, and then immediately is capable of delivering to that demand. Also, it is unnecessarily conservative to assume that the IR drop is the full drop the whole period in which the capacitor discharges as the current drops as the capacitor discharges. To analyze the power distribution system in more detail requires running a simulation from the power source model to the Pentium Pro processor power model, including all board, cable, and capacitor effects. See Section 7.5 for more information on component models and Section 11 for the Pentium Pro processor power model.

4.3.2. HIGH FREQUENCY DECOUPLING

Since the bulk storage not only contains an effective series resistance, but also a fairly high inductance, these capacitors need to be assisted by other capacitors that have a lower inductance (but typically less capacitance). These *high frequency* capacitors will control the switching transients and hold-over the power planes during an average load change until the higher inductance capacitors can react.

The 1206 surface mount package is a fairly low inductance package, and is actually lower than the inductance of an 0603 package due to the geometry of the board interconnects. For even lower inductance one can use a 0612 package since the board interconnect area gets even larger. An 0612 is the same size as the 1206 but has its pads along the long edge. The cost of these is significantly higher however due to the complexity of mass producing them. The 1206 package capacitors on the other hand are readily available and low cost.

One difficulty in simulating with high frequency capacitors however, is that vendors do not readily offer a specification for the inductance of their parts. In Section 7.5 are some measured values from capacitors that Intel has investigated which should be verified against the vendors' parts that will actually be used in any design. After calculating the number of capacitors required, one can look at the impact that averaging tolerances over many measured components has to the design and pad the design appropriately with additional components.

Since the capacitor inductance is package related, choose the largest value available in the package that has been chosen. The highest capacitance obtainable will be the most beneficial for the design since the amount of capacitance behind this inductance is still critical.

This simple law of inductance is useful for estimating the number of high frequency capacitors required:

Equation 6. Simple Law of Inductance

$$V = L\, di/dt$$

V is the voltage drop that will be seen due to the inductance. A di/dt value of 0.3A/ns can be used to estimate the Pentium Pro processor and L is the inductance of a series combination of via, trace, and all of the high frequency capacitors in parallel. See Section 4.4 for ideas on reducing via and trace inductance.

Once the allowable inductance for the budgeted voltage drop (due to high frequency transitions) is calculated, the number of capacitors (N) required can be estimated by:

Equation 7. Number of Capacitors Required

$$N = L_n / L$$

where L_n is the inductance of a single capacitor and L is the inductance required that was calculated above.

For example, to meet a 0.3A/ns di/dt and not produce more than 60 mV of noise due to high frequency capacitor inductance (1.9 nH from Table 5) one would simply plug into Equation 6 and Equation 7.

Equation 8. Inductance Allowed

$$L = 0.060V \div 0.3\,A/ns = 0.2nH$$

Equation 9. Number of Capacitors for 0.2 nH

$$N = 1.9nH \div 0.2nH = 10 capacitors$$ [1]

Footnote

[1] More capacitors will actually be required to achieve the necessary capacitance prior to the voltage regulator module due to the limited space within a 1206 package. The number of capacitors required for a Pentium Pro processor is therefore "capacitance dependent".

Resistance of the high frequency capacitors can also be included in the above analysis, but the resistance and current for each capacitor are low enough that this should not be necessary.

While the above calculation provides a theoretical number of capacitors required to meet the processor di/dt requirements, high frequency noise may yet persist. More capacitors may be necessary to control noise from other sources. However, mixing additional values in the design to create higher resonance points should not be useful since the capacitors described (1206 package) have very high resonant frequencies already. This is shown by using the values from Table 5 in Equation 10.

Equation 10. Resonant Frequency

$$f = \frac{1}{2\pi\sqrt{LC}} \approx \frac{1}{2\pi\sqrt{(0.47\times10^{-9})\times(1\times10^{-6})}} \approx 7.3MHz$$

Note that all 1206 capacitors will have basically the same inductance value and that smaller components actually have more inductance. Also, the inductance of the vias are the larger contributors and actually cause the resonance to be more like 3.6 MHz .

4.4. Power Planes or Islands

The imperfections of the power planes themselves have so far been ignored. These may also introduce unwanted resistance and inductance into the power distribution system. In the complex model in Figure 3 these imperfections are referred to as R_{BOARD} and L_{BOARD}.

Power should definitely be distributed as a plane. This plane can be constructed as an *island* on a layer used for other signals, on a supply plane with other power islands, or as a dedicated layer of the Printed Circuit Board (PCB). Processor power should never be distributed by traces alone. See Figure 20 for an example of a voltage island.

Due to the fact that the Pentium Pro processor voltage is unique to most system designs, a voltage island, or islands, will probably be the most cost effective means of distributing power to the processors. This island should be continuous from the source of power to the load. It should also completely surround all of the pins of the source and all of the pins of the load.

Figure 20 also shows the placement of an SMA-type coaxial connection. This connection will later allow the direct connection of an oscilloscope for accurate power plane measurements.

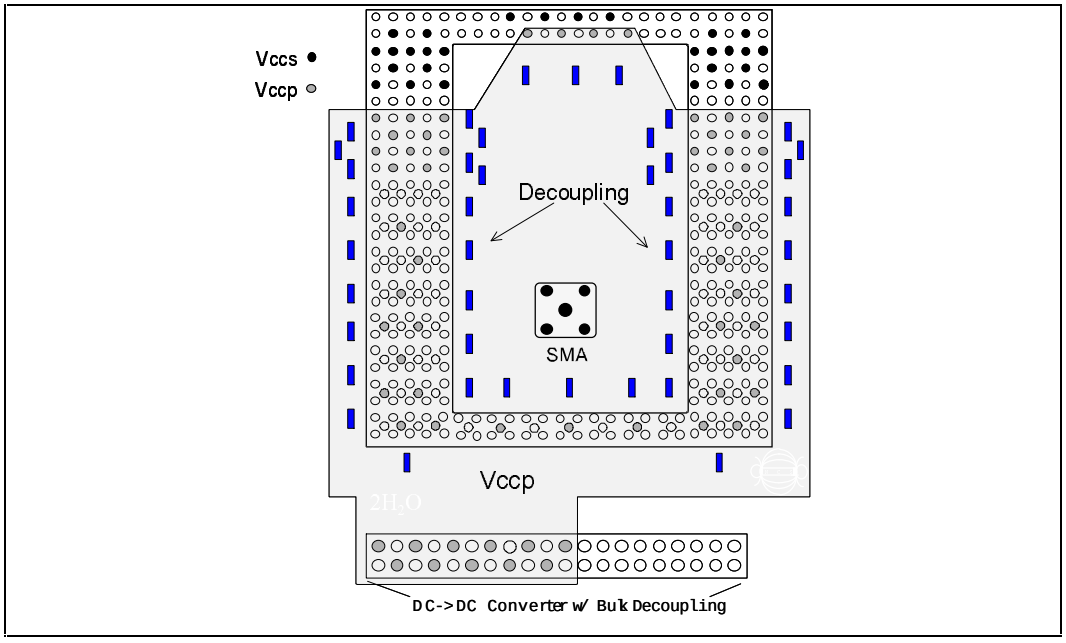

Figure 20. A Pentium® Pro Processor Voltage Island

4.4.1. LOCATION OF HIGH FREQUENCY DECOUPLING

High frequency decoupling should be placed as close to the power pins of the load as physically possible. Use both sides of the board if necessary for placing components in order to achieve the optimum proximity to the power pins. This is vital as the inductance of the board's metal plane layers could cancel the usefulness of these low inductance components.

Another method to lower the inductance that should be considered is to shorten the path from the capacitor pads to the pins that it is decoupling. If possible, place the vias connecting to the planes within the pad of the capacitor. If this is not possible, keep the traces as short as is feasible. Possibly one or both ends of the capacitor can be connected directly to the pin of the processor without the use of a via. Even if simulation results look good, these practical suggestions can be used to create an even better decoupling situation where they can be applied in layout. Figure 21 illustrates these concepts.

4.4.2. LOCATION OF BULK DECOUPLING

The location of bulk capacitance is not as critical since more inductance is already expected for these components. However, knowing their location and the inductance values involved will be useful for simulation. In this example the bulk capacitance is on the voltage converter module electrically *behind* the inductance of the converter pins. This is Intel's recommended solution.

4.4.3. IMPEDANCE AND EMISSION EFFECTS OF POWER ISLANDS

There are impedance consequences for signals that cross over or under the edges of the power island that exists on another layer. While neither of these may be necessary for most designs, there are two reasonable options to consider which can protect a system from these consequences.

The Pentium Pro processor power islands can be isolated from signals by one of the solid power plane layers such as the ground layer. This forces a particular stack-up model.

Another option that helps, but does not completely eliminate radiation effects, is to decouple the edges of the CPU power islands to ground on regular intervals of about 1" using good high frequency decoupling capacitors (1206 packages). This requires more components but does not require any particular board stack-up.

In either event, for controlling emissions, all planes and islands should be well decoupled. The amount of decoupling required for controlling emission will be determined by the exact board layout, and the chassis design. One should plan ahead by allowing additional pads for capacitors to be added in case they are discovered necessary during initial EMI testing.

5.0. THE GTL+ BUS POWER REQUIREMENTS

The GTL+ bus is an end terminated, open-drain bus. Both ends are terminated to a voltage level called V_{TT} (1.5V) which becomes a supply of current when output drivers are turned on. There are approximately 150 GTL+ lines in a Pentium Pro processor system design.

The GTL+ bus power requirements present a different situation than creating power for the CPUs. While the current required is less than that for a processor, the GTL+ bus does have a fairly tight tolerance specification. Just as the processor can start and stop executing within a few clock cycles, the bus usage follows, which in turns causes load changes and transients on the GTL+ power supply (V_{TT}). Since the GTL+ bus is terminated at both ends, V_{TT} must be available to the termination resistors at both ends of the bus. This can be accomplished by having two sources of V_{TT} or by distributing V_{TT}.

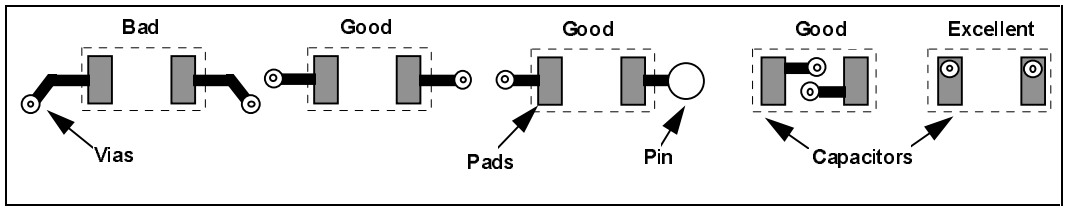

Figure 21. 1206 Capacitor Pad and Via Layouts

Table 4. Estimating V_{TT} Current

Signal Group	Quantity of Signals	Maximum Duty Cycle	Average Current
Data + ECC	72	100	3.24
Address + Parity	35	67	1.06
Arbitration	7	100	0.32
Request	7	67	0.21
Error	5	20	0.05
Response	6	33	0.09
Other	9	100	0.41
Total	141		5.38

The maximum current that a GTL+ buffer will sink is 45 mA. When considering the duty cycle of the signals, the maximum current that the 141 signals will draw is about 5.38 Amps at 100% utilization of the bus. Notice that the duty cycles are chosen rather conservatively in Table 4. The actual current will be limited by the utilization of the bus and by the value of the termination resistors in the design. These benefits can be taken into account as well.

5.1. Tolerance

The tolerance specification is 150 mV. It is again important to note that this tolerance specification covers all voltage anomalies including power supply ripple, power supply tolerance, current transient response, and noise. Not meeting the specification on the low or high end will change the rise and fall time specifications. Failure to meet this specification on the low end will also result in reduced margins for the GTL+ buffers thus making it more difficult to meet timing specifications.

5.2. Reference Voltage

The GTL+ bus requires a Voltage Reference called V_{REF} as well. V_{REF} is to be set at 2/3 V_{TT}. The current draw on this signal is very low (at most 15µA per device) and can be created by a simple voltage divider of two resistors. Bear in mind that the leakage current can vary and may be significant when building the voltage divider.

6.0. MEETING THE GTL+ POWER REQUIREMENTS

Due to the different nature of powering the GTL+ bus versus powering a processor, meeting the V_{TT} requirements may be addressed in a different way.

6.1. Generating V_{TT}

Since the GTL+ bus must be terminated on both ends of the bus, it may be convenient in many designs to generate V_{TT} on each end of the line. Each will only be required to supply one half of the current necessary to the GTL+ drivers. If both ends of the bus are fairly near each other, then one supply could suffice.

When powering the bus from a single regulator, the techniques of design will closely resemble those of Section 4 and a full analysis should be run.

When powering each end of the bus separately, the current will be low enough that a linear regulator can reasonably be used to generate it. Linear regulators are faster devices than switching regulators and will therefore require less output decoupling. Also, due to the lower current, the ESR and ESL of components will not be as large an issue as before. A proper analysis as in described in Section 4 could be considered. The techniques would remain the same, while the reaction time of the supply and the current levels will be different.

It is not necessary for these two regulators to track each other as long as each maintains the specification on V_{TT}. The bus will naturally perform an averaging function on these two inputs which must also be followed by V_{REF} as discussed in Section 6.3.

6.2. Distributing V_{TT}

V_{TT} is only needed at the termination resistors and for generation of V_{REF}. If the distance to the termination resistors is small, distributing V_{TT} with a wide trace should be sufficient. The trace to the V_{REF} generation

point should also be wide, even though the current is low, in order to keep its inductance minimal.

If one source of the V_{TT} voltage is used to power both ends of the bus, and the ends are not near each other, then a plane may be useful for V_{TT} distribution. This will help offset the resistive and inductive losses that are an issue for V_{TT} distribution just as they are issues for $V_{CC}P$. Separate smaller linear regulators at each end of the bus may alleviate the possible need for a power plane.

NOTE

When using resistor networks with single corner pin V_{cc} connections for GTL+ termination, beware of inductive packages. Intel has found that these packages can cause significant voltage drops due to the inductance in the 24 pin SOIC packages being used for this purpose.

6.3. Generating and Distributing V_{REF}

V_{REF} is a low current input to the differential receivers within each of the components on the GTL+ bus. As it is fairly low current (at most 15µA per device), it can be generated by a simple voltage divider. Because V_{REF} is used only by the input buffers, it does not need to maintain a tight tolerance from component to component. It does however need to meet the 2% specification at all V_{REF} inputs and should track the V_{TT} averaging that occurs if using two regulators at opposite ends of the bus.

The V_{REF} specification is 2/3 V_{TT} ± 2%. By using 1% resistors one can easily meet this specification. In Figure 22, using $R_1 = 2 \times R_2$, V_{REF} is set at a nominal value of 2/3 V_{TT}.

Equation 11. Creating V_{REF} of 2/3 V_{TT}

$$V_{REF} = V_{TT} \times \frac{R_1}{R_1 + R_2} = V_{TT} \times \frac{2 \times R_2}{2 \times R_2 + R_2} = \tfrac{2}{3} V_{TT}$$

R_1 and R_2 should be small enough values that the current drawn by the V_{REF} inputs (I_{REF}) is negligible versus the current caused by R_2 and R_1.

A complete analysis of this circuit's currents into and out of the center node, as in Equation 12, will provide the final V_{REF} of the circuit. *n* is the number of I_{REF} inputs supplied by the divider.

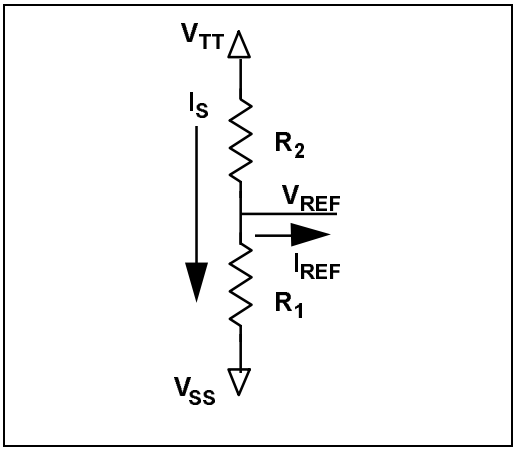

Figure 22. V_{REF}

Equation 12. Node Analysis

$$I(R_2) = I(R_1) + n \times I_{REF}$$

Plugging in for the currents and rearranging, gives:

Equation 13. Node Analysis in Terms of Voltage

$$\frac{V_{TT} - V_{REF}}{R_2} - \frac{V_{REF}}{R_1} = n \times I_{REF}$$

Which leads to:

Equation 14. Solving for V_{REF}

$$V_{REF} = \frac{V_{TT}/R_2 - n \times I_{REF}}{1/R_2 + 1/R_1}$$

The worst case V_{REF} should be analyzed with I_{REF} at the maximum and minimum values determined for the number of loads being provided voltage. If the number of loads can change from model to model or because of upgrades, this should be taken into account as well. Equation 14 should also be analyzed with R_1 and R_2 at the extremes of their tolerance specifications.

6.3.1. DISTRIBUTING V_{REF} OR V_{TT}

A resistor divider can be placed at each component by distributing V_{TT}, or V_{REF} can be generated at a voltage regulator and then distributed to each of the devices. To eliminate noise and losses on whichever level is distributed, use a wide isolated trace. The current should be fairly low in either case, but this extra width will help keep the induced noise level down.

If more than one regulator is being used to generate V_{TT}, then V_{REF} must track them by averaging from both V_{TT} sources. One method of accomplishing this is to generate a separate V_{REF} at each regulator for up to four loads each, and then connect the two together with a wide trace. The closer this V_{REF} signal tracks the path of the bus signals, the better it will match the averaging of the voltage on the GTL+ bus. However, this signal should be routed on a separate layer in order to keep cross-talk off of it.

7.0. RECOMMENDATIONS

Designing and verifying one's own system using simulation is highly recommended. With the above estimates, a model of the power source, and the provided model of the Pentium Pro processor in Section 11, analog modeling can be started. Intel recommends the following as a starting point, or benchmark.

7.1. $V_{CC}S$

For $V_{CC}S$, use a standard PC power supply with a 3.3V tap. Be sure that there is sufficient current on the 3.3V tap of the supply to power all of the system chipset, the GTL+ regulator (if run off of 3.3V), other 3.3V logic in the system and any possible L2 caches that may someday exist in the system. See the chipset specification for chipset power requirements. See the *flexible motherboard* specifications in the *Pentium® Pro Processor Developer's Manual, Volume 1* for the requirements of the L2 cache. Bulk decoupling requirements will be highly dependent on the reaction time of the power supply that is chosen. For high frequency decoupling, twenty (20) 0.1µF capacitors in a 1206 package should be more than adequate. This should limit di/dt noise to 20 mV. While this sounds extravagant, it is wise to keep L2 noise isolated from other components that will be sharing the 3.3V supply, and vice versa. Note that no decoupling is required when supporting only processors in which the L2 receives power from the $V_{CC}P$ pins.

7.2. $V_{CC}P$

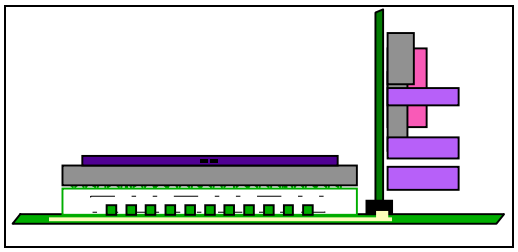

Figure 23. Local Regulation

For $V_{CC}P$, Intel recommends starting with a socketed local DC-to-DC converter as shown in Figure 23. This removes cable inductance from the distribution, reduces board inductance, and allows for a low cost upgrade strategy as well. Regulator sockets can be provided for upgradable processor sockets rather than shipping with the full current capability already available. Another benefit of using separate regulators per processor is the ability to mix and match processor types in the system. The output of this regulator should be adjustable to allow for changes in the voltage specification as new products become available.

Section 10 discusses recommended specifications for the DC-to-DC converter. These specifications have been provided to the DC-to-DC converter industry.

Intel recommends that the bulk decoupling be placed on this DC-to-DC converter module. Since these capacitors tend to be large and not available in surface mount technology, it makes sense to isolate these to a smaller module that can be run in a different manufacturing environment than the typical system board designs. Up to fourteen (14) 1000µF Electrolytic capacitors with an ESR of less than 55 mΩ each should be placed **on the converter module**, depending on the switching rate of the converter.

The high frequency decoupling should be composed of at least forty (40) 1.0µF capacitors in the 1206 package. Ten or more are needed to meet the inductance requirements and 40µF is required to slow the di/dt to 30A/µs for the DC-to-DC converter specification. These should be placed close to the $V_{CC}P$ pins as shown in Figure 20. An open centered socket will make this job easier and allow for the use of the space immediately under the processor. The plane can be constructed as an island as in Figure 20 without any special isolation from the signal layers.

7.2.1. THE MAIN POWER SUPPLY

The main supply must be able to provide power to the DC-to-DC converter as well as to the rest of the system. One should ensure that the input voltage to the converter meets the converter's requirements, and that the DC-to-DC converter does not create a transient problem of its own on the 5V or 12V outputs of the main supply. The guidelines that were given to the DC-to-DC converter industry are described in Section 10.2, and should be checked against the supply that is planned for the system. For example, the current slew rate capability of the power supply voltage to the regulator may be 0.2 Amp/μs with 10,000μF of load.

7.3. V_{TT}

Intel recommends supplying V_{TT} to each end of the GTL+ bus using a separate linear regulator for each end. Since the losses in a linear regulator are directly proportional to V_{IN}-V_{OUT}, the 3.3V power supply makes a good choice for the input voltage to the regulator. The CPU voltage may seem like a better choice if it is lower than 3.3V, but it will be varying from one Pentium Pro processor variant to the next. This may cause a design change for each generation of Pentium Pro processor. Also, Linear regulators require a minimum voltage drop in order to operate which may become an issue as the Pentium Pro processor voltage decreases.

By using separate linear regulators, the voltage distribution is contained to a very local region. In a bus layout where both ends of the bus are physically near each other, one regulator can be used to supply both sets of termination resistors. In this situation, a 50 mil trace (The wider the better) should be sufficient for distributing the power to the termination resistors.

Linear regulators are fairly common and produced by many vendors. See your local field applications engineer for assistance locating a vendor.

Bulk capacitance for the regulator will be determined from the reaction time specifications of the regulator chosen. The capacitance must be enough to hold-over the regulator during a switch from 0 to 5.4 Amps, as estimated in Table 4, until the regulator reacts. In addition, ten 1.0μF capacitors are recommended for high frequency decoupling on each end of the Pentium Pro processor bus. These should be distributed as near to the termination resistors as possible.

7.3.1. TERMINATION RESISTORS

Discrete resistors may be employed, however the assembly time associated with placing about 280 resistors should be taken into account. A lower part count implementation uses resistor networks.

NOTE

When using resistor networks with single corner pin VCC connections for GTL+ termination, beware of inductive packages. Intel has found that these packages can cause significant voltage drops due to the inductance in the 24 pin SOIC packages being used for this purpose. A better option is to use resistor networks in which both ends of each resistor are available as pins.

7.4. V_{REF}

Intel recommends one voltage divider at each component, or at a minimum, one voltage divider at each regulator. One per component means that V_{REF} won't need to be distributed.

The rest of this discussion addresses how to design for one voltage divider at each regulator, since the same resistor values can be used when there is one voltage divider per component. Note that all V_{REF} inputs of one component should be tied together, and can be counted as one load. Each load is specified at a maximum of 15 μAmps of leakage current which makes four loads (For one voltage divider supplying 4 loads of an 8 load system) a maximum of 60 μAmps per voltage divider. Note that these leakage currents can be positive or negative.

Using 1% resistors for the voltage divider in Figure 24, make R_1 a 150Ω resistor, and use 75Ω for R_2 . This will create a static usage of 7 mA (1.5V/225Ω) per voltage divider. After looking at all combinations of R_1 and R_2 (above and below tolerance) and I_{REF} (±60μA), the worst case solution for Equation 14 can be found with I_{REF} at 60μAmps, R_1 at the low end of its tolerance specification (148.5Ω), and R_2 at the high end of its tolerance specification (75.75Ω). This yields:

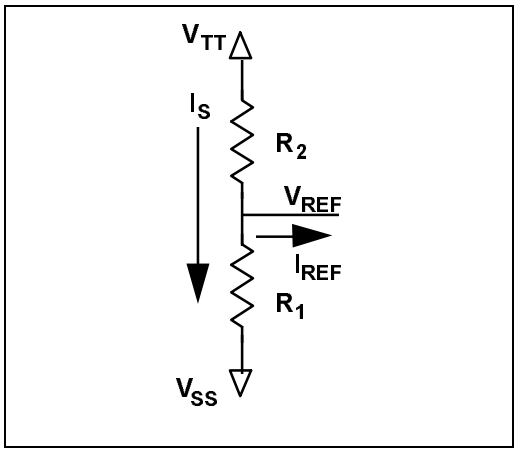

Figure 24. Generating V_{REF}

Equation 15. Resistor Tolerance Analysis

$$V_{REF} = \frac{1.5/75.75 - .000060}{1/75.75 + 1/148.5} \approx 0.99V$$

Since the target of 2/3 of V_{TT} is 1.00V, this setting is within 0.97% of the 2/3 point and satisfies the 2% specification. The other corners can be easily verified by the reader through the use of a spreadsheet program. V_{TT} can also be varied over its tolerance range, but this effect is minimal.

These values chosen for R_1 and R_2 have additional benefits. The parallel combination terminates the V_{REF} line to 50 ohms, and both are standard values of resistors which should benefit their cost.

V_{REF} should be decoupled with a 0.001 µF capacitor to V_{SS} located at each V_{REF} input and at the voltage divider. At the voltage dividers, V_{REF} can also be decoupled with a 0.001 µF capacitor to V_{TT} to further enhance the ability for V_{REF} to track V_{TT}. The actual benefit of this controversial.

When routing V_{REF} to the loads, use a 30-50 mil trace (The wider the better) and keep all other signals at least 20 mils away from the V_{REF} trace. This will provide a low impedance line without the cost of an additional plane or island.

Finally, if generating V_{REF} at the voltage regulators, both V_{REF} levels should be tied together in order to provide an automatic averaging across all devices to match the natural averaging that occurs between the two regulators over the GTL+ bus signals. If possible, use a separate layer from the GTL+ signal layers and follow the path of the bus signals. This will provide the best averaging effect.

7.5. Component Models

Component models should be acquired from the manufacturers. Intel can not guarantee the specifications of another manufacturer's components. This section contains some of the models that Intel has developed for its simulations. The Pentium Pro processor model can be found in Section 11.

Table 5. Various Component Models Used at Intel (Not Vendor Specifications)

Component of Simulation	ESR (Ω)	ESL (nH)	ESL+ Trace + Via (nH)
0.1µF Ceramic 0603 package	0.100	1.60	3.0
1.0µF Ceramic 1206 package	0.120	0.47	1.9
100µF MLC (2.05"x0.71")	0.005	0.30	1.7
47µF, 16V Tantalum D Case	0.100	0.602	2.0
330µF, 16V Aluminum Electrolytic	0.143	2.37	3.8
1000 µF, 10V Aluminum Electrolytic (20mm)	0.053	N/A	N/A
1000 µF, 25V Aluminum Electrolytic (25mm)	0.031	N/A	N/A
L_{BOARD}. One used for V_{SS}, one for $V_{CC}P$. This estimate accommodates traces to vias, planes and the socket connections to the plane.	0.000	0.40	N/A

8.0. MEASURING TRANSIENTS

In order to measure transients on a voltage island, a clean connection will be required. A good way to achieve this is by the placement of a coaxial connection directly into the power island during layout. An SMA type connector can be used and should be placed near the centrum of the array of pins receiving that voltage as in Figure 20.Since a cable will mate to this connector while the system is functioning, this connector must be placed on the opposite side of the board as the processor.

Cable the signal directly into the oscilloscope and take the reading with the oscilloscope bandwidth limited to 20MHz. This will filter out the components of the Vcc noise that the package characteristics also filter out. There is no need to decouple frequencies above this range since these frequency components will not enter the Pentium Pro processor package.

9.0. EXISTING TECHNOLOGY FOR A PENTIUM® PRO PROCESSOR SYSTEM DESIGN

9.1. Solutions for $V_{CC}P$

Intel has assisted in the development of many industry DC-to-DC Converter modules for the Pentium Pro processor. Any of these components used in a specific design should be understood by the designer and can not be guaranteed by Intel for use in that design. In general, the vendor of any component will assist in the usage of their component. See your local field office for a list of possible vendor solutions.

Another solution that is a simple extension to the discussion in this paper is to integrate the components of the DC-to-DC converter, including the bulk capacitance, onto the system PCB. Intel has helped power silicon vendors as well in designing Pentium Pro processor specific solutions. Again, see your local field office for a list of possible vendor solutions.

9.2. Linear Regulators for V_{TT}

Linear regulators are widely available. Switching regulators can also be used to generate V_{TT}.

9.3. Termination Resistors

Intel recommends the use of resistor networks to reduce the part count of the processor board assembly. The best options are resistor networks with separate pin access to each side of every resistor in the package. This will minimize any inductance or crosstalk within the package.

When using resistor networks with single corner pin V_{CC} connections for GTL+ termination, beware of inductive packages. Intel has found that these packages can cause significant voltage drops due to the inductance in the 24 pin SOIC packages being used for this purpose.

10.0. DC-TO-DC CONVERTER SPECIFICATIONS

The following specifications define DC-to-DC converters to meet the requirements of the Pentium Pro processor and future Intel microprocessors.

Each specification is placed into one of three categories:

REQUIRED: An essential part of the design; cannot meet minimum Pentium Pro processor specifications without it.

EXPECTED: Part of Intel's standard Pentium Pro processor power definitions; necessary for consistency with the designs of many systems and power devices. Required by most Pentium Pro processor flexible motherboard designs.

GUIDELINE: Normally met by of this type of DC-to-DC converter and, therefore, included as a design target. Likely to be specified by system manufacturers.

10.1. Electrical Specifications

Specification Summary **REQUIRED**

The DC-to-DC converter must meet the specifications for any processor it is intended to power in a system. For example, Table 6 shows the specifications for a DC-DC converter to support a 150 MHz Pentium Pro processor with a 256-Kbyte L2 cache. Converters supporting the requirements of a Pentium Pro processor flexible motherboard must meet the broader requirements of Table 8.

Table 6. 150 MHz, 256-Kbyte L2 Cache Pentium Pro® Processor Voltage and Current Specifications

Parameter	Value
Voltage	3.1V ± 5%
Current	0.3 - 9.9A
Slew rate	30A/μs at converter pins

10.1.1. INPUT VOLTAGES

Available inputs are at 12V ±5% and at 5V ±5%. Either one or both of these inputs may be used by the converter. The vendor must provide maximum current loading requirements on all inputs. These voltages are supplied by a conventional PC power supply through a cable to the motherboard.

Load Transient Effects on Input Voltages **GUIDELINE**

The converter must be able to provide for an output current step at the load from I_{MIN} to I_{PEAK} (per Table 7) in 360 ns. During this step response the input current di/dt must not exceed 0.1 Amps/μs. For applications with multiple converters, it is recommended that the step response di/dt of an individual converter not exceed 0.04 Amps/μs.

10.1.2. I/O CONTROLS

These are signals that control the DC-to-DC converter or provide feedback from the DC-to-DC converter (shown with corresponding pins in Table 10). Input and output levels must be consistent with TTL DC specifications.

Power-Good (PWRGD) **GUIDELINE**

An open collector signal must be provided. When the output voltage is not within specifications (nominal or selected voltage ±10%) this signal must be at the low state. This signal must transition to the proper state within 5 milliseconds of the output coming into or going out of its specified range.

Output Enable (OUTEN) **GUIDELINE**

The module must accept an open collector signal for controlling the output voltage: The low state must disable the output voltage. When disabled, the PWRGD output must be in the low state.

Upgrade Present (UP#) **EXPECTED**

The module must accept an open collector signal, used to indicate the presence of an upgrade processor. Typical state is high (standard processor in system). When in the low or ground state (OverDrive processor in system) the output voltage must be disabled unless the converter can supply to an OverDrive processor's specifications (see Table 8). When disabled, the PWRGD output must be in the low state.

Voltage Identification (VID[0:3]) **EXPECTED**

The module must accept four signals, used to indicate the voltage required by the processor, as defined by Table 9.

10.1.3. OUTPUT REQUIREMENTS

DC Output Current **REQUIRED**

The DC output current requirements corresponding to the processor in Table 6 are shown in Table 7.

Table 7. DC Output Current

Parameter	Value
I_{MIN}	0.3 Amps
I_{MAX}	9.9 Amps
I_{PEAK} (Several μs of overshoot)	11 Amps

Voltage Range by Application **EXPECTED**

A Pentium Pro processor-based system may require one of the adjustment ranges shown in Table 8. The I_{CC} column represents the current requirement Intel expects for processors at each voltage.

Processor Voltage Identification **EXPECTED**

The adjustment mechanism must be by four binary weighted inputs using the coding described in Table 9.

Four Pentium Pro processor pins will have an open–ground pattern corresponding to the voltage required by the individual processor unit. Voltages outside of the 2.4-volt to 3.5-volt range may be considered optional for use by the module supplier and system manufacturer.

Table 8. Voltage Ranges

Application Support	V_{MIN}	V_{MAX}	I_{CC}
Pentium® Pro processor	2.9 Volts	3.5 Volts	(up to) 13 Amps
Pentium Pro processor + OverDrive® Processor Upgrade	2.4 Volts	3.5 Volts	13 Amps

Table 9. Voltage Identification Code

Pentium® Pro Processor Pins				$V_{CC}P$
VID3	VID2	VID1	VID0	(VDC)
1	1	1	1	No CPU
1	1	1	0	2.1
1	1	0	1	2.2
1	1	0	0	2.3
1	0	1	1	2.4
1	0	1	0	2.5
1	0	0	1	2.6
1	0	0	0	2.7
0	1	1	1	2.8
0	1	1	0	2.9
0	1	0	1	3.0
0	1	0	0	3.1
0	0	1	1	3.2
0	0	1	0	3.3
0	0	0	1	3.4
0	0	0	0	3.5

NOTES:

0 = Processor pin connected to V_{SS}

1 = Processor pin open (system design may include pull-up resistor to voltage consistent with TTL input levels)

DC Voltage Regulation **REQUIRED**

Voltage regulation limits must include:

- Output load ranges specified in Table 8.
- Output ripple/noise.
- DC Output initial voltage set point adjust
- Temperature and warm up drift specified in Table 11.
- Output load transient (slew rate) as defined in Table 6.

The toggle rate for the output load ranges specified in this section must range from 100 Hz to 100 kHz. Under the above conditions and for all toggle rates, voltage levels must be ±5% of nominal setting, as measured over a 20 MHz frequency band.

Output Ripple and Noise **GUIDELINE**

Ripple and noise are defined as periodic or random signals over the frequency band of 20 MHz at the output pins. Output ripple and noise requirements of ±1.0% must be met throughout the full load range and under all specified input voltage conditions.

Variation with Load **GUIDELINE**

To assist in providing margin during high slew rate current load transitions, the vendor may target module performance so as to provide for a nominal +2% offset when under minimum load conditions, and a nominal -2% offset when under maximum load conditions.

Overshoot At Turn-On/Turn-Off **GUIDELINE**

Overshoot upon the application or removal of the input voltage under the conditions specified in this section must be less than 10% above the initial set output voltage. No voltage of opposite polarity must be present on any output during turn-on or turn-off.

Turn-on Response Time **GUIDELINE**

The output voltage must reach 99% of nominal level within 10 ms of the input reaching 90% of nominal level.

Efficiency **GUIDELINE**

The efficiency of the DC-to-DC converter must be greater than 80% at high current draw and greater than 40% at low current draw.

10.1.4. PROTECTION

These are features built in to the DC-to-DC converter to prevent damage to itself or the circuits it powers.

Over-Voltage Protection (OVP) **GUIDELINE**

Protection level: The converter must provide over-voltage protection by shutting itself off when the output voltage rises beyond V_{TRIP}. V_{TRIP} must be set between 10% and 20% above the selected output voltage level.

Short Circuit Protection **GUIDELINE**

A load short circuit is defined as a load impedance of less than approximately 200 mΩ. The DC-to-DC converter must operate in a constant current mode for a shorted output. The DC-to-DC converter must be capable of withstanding a continuous short-circuit to the output without damage or over-stress to the unit.

Reset After Shutdown **GUIDELINE**

If the DC-to-DC converter goes into a shutdown state due to a fault condition on its outputs, the DC-to-DC converter must return to normal operation after the fault has been removed, or after the fault has been removed and power has been cycled off and on.

Voltage Sequencing **REQUIRED**

No combination of input voltages may falsely trigger an OVP event.

10.2. Mechanical Requirements

10.2.1. PHYSICAL DESCRIPTION

Dimensions **EXPECTED**

Outline dimensions must be equal to or less than 3.1” x 1.5” x 1.0”. Maximum component height must be 0.80" on the connector side and 0.14" on the back side of the module. Figure 26 shows the outline of a module board.

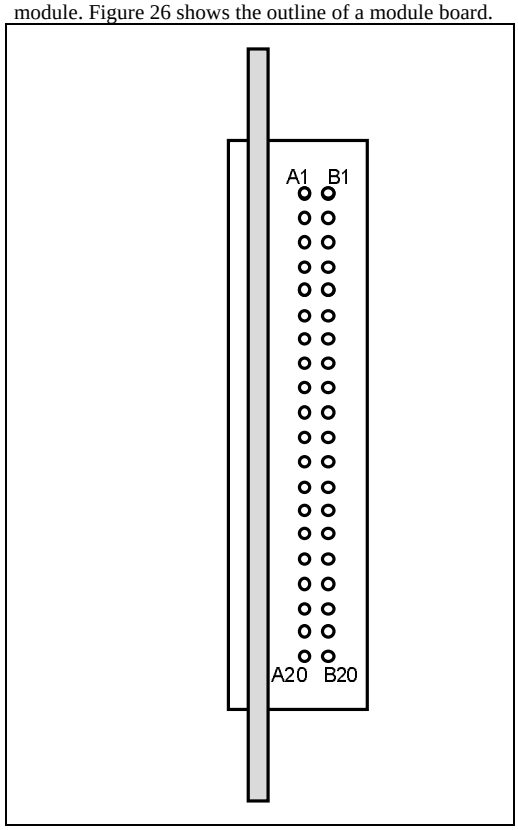

Figure 25. Pin Orientation (Top View)

Interconnect **EXPECTED**

Interconnect must consist of a 40 pin interface with the socket (type AMPMOD2, part number 532956-7, or equivalent) mounted to the module. Figure 25 shows the pin orientation of the DC-to-DC converter, and Figure 27 shows the connector features. The baseboard interface pins must conform to Intel’s *Voltage Regulator Module 8 Header, Revision 3.0* (VRM 8, see Figure 28). The current capacity must be at least 2 Amps/pin. The pin electrical interface is given in Table 10.

Table 10. Pin Definitions

Pin #	Row A	Row B
1	$5V_{IN}$	$5V_{IN}$
2	$5V_{IN}$	$5V_{IN}$
3	$5V_{IN}$	$5V_{IN}$
4	$12V_{IN}$	$12V_{IN}$
5	$12V_{IN}$[1]	Reserved
6	Reserved	OUTEN
7	VID0	VID1
8	VID2	VID3
9	UP#	PWRGD
10	$V_{CC}P$	V_{SS}
11	V_{SS}	$V_{CC}P$
12	$V_{CC}P$	V_{SS}
13	V_{SS}	$V_{CC}P$
14	$V_{CC}P$	V_{SS}
15	V_{SS}	$V_{CC}P$
16	$V_{CC}P$	V_{SS}
17	V_{SS}	$V_{CC}P$
18	$V_{CC}P$	V_{SS}
19	V_{SS}	$V_{CC}P$
20	$V_{CC}P$	V_{SS}

NOTE:

- Connection to A5 is optional for a 12V input of less than 4 Amps.

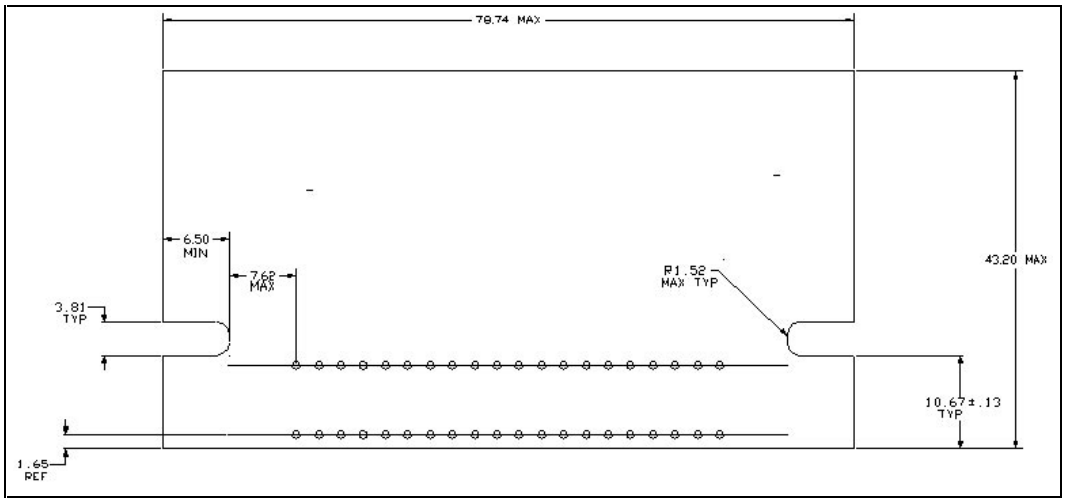

Figure 26. Module Printed Wiring Board (Dimensions in mm)

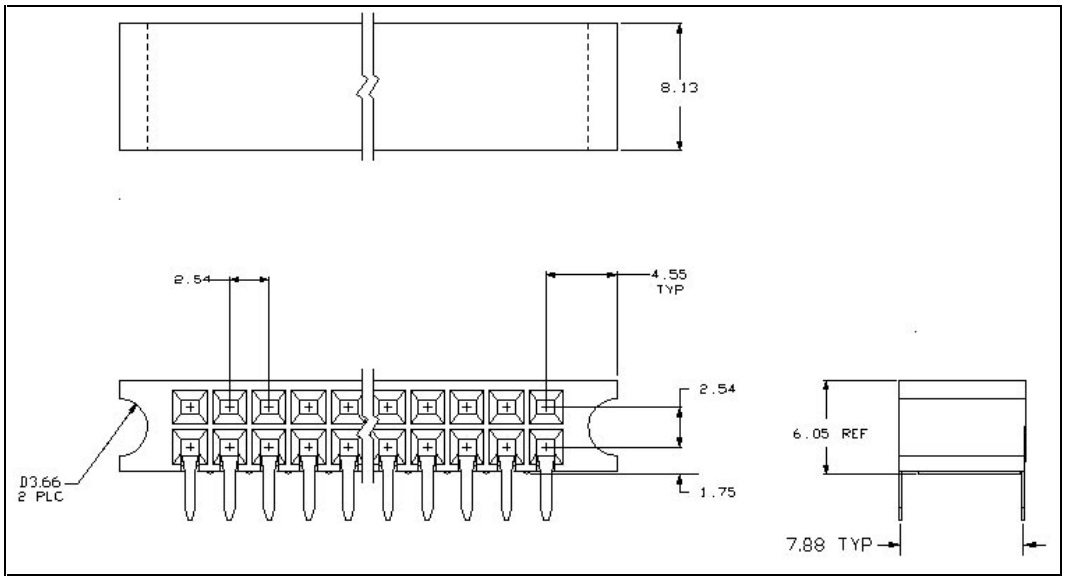

Figure 27. Module Connector Features (Dimensions in mm)

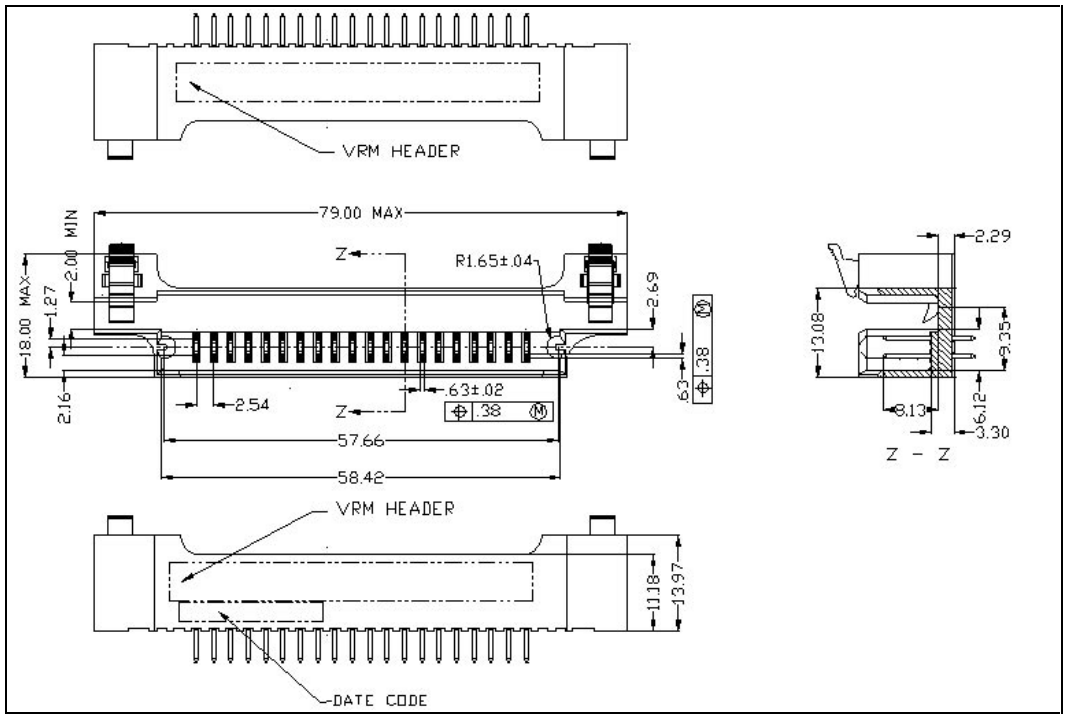

Figure 28. Mating Header (Dimensions in mm)

Weight **EXPECTED**

Package weight, including any integral heat sink, must be less than three ounces.

10.2.2. MECHANICAL INTERFACE

Mating Header **REFERENCE**

The VRM 8 Header (see Figure 28) is a 40-position, two-row, shrouded header with straight posts on 0.1 inch centers (AMP part number 146315-1 or equivalent). The complete, current VRM 8 specification is available from Intel's End User Component Division (OverDrive Processors).

Baseboard Attachment **EXPECTED**

The voltage regulator module is to be retained to and removed from the header by features on the header that mate with the voltage regulator module. The removal and installation process must not require the use of tools. The removal features must be accessible from the back side (opposite the receptacle) of the module.

Alternative Baseboard Attachment **REFERENCE**

An alternative mounting configuration is shown Figure 29. In this configuration the baseboard interface must be a non-shrouded connector (type AMPMOD2, part number 2-103783-0 or equivalent). This mounting configuration is recommended for applications where, under normal usage, the module would not be removed after installation.

10.3. Tests and Standards

Environmental GUIDELINE

Design, including materials, must be consistent with the manufacture of units that meet the environmental standards in Table 11.

Table 11. Environmental Guidelines

	Operating	Non-Operating
Temperature	Ambient +10°C to +60°C at full load with a maximum rate of change of 5°C per 10 minutes minimum but no more than 10°C per hour	Ambient –40°C to 70°C with a maximum rate of change of 20°C/hour.[1]
Humidity	To 85% relative humidity.	To 95% relative humidity.
Altitude	0 to 10,000 feet	0 to 50,000 feet.
Electrostatic discharge	15 KV initialization level. The direct ESD event must cause no out-of-regulation conditions.[2]	25 KV initialization level.

NOTES:

1 Thermal shock of –40°C to +70°C, 10 cycles; transfer time must not exceed 5 minutes, duration of exposure to temperature extremes must be 20 minutes.

2 Includes overshoot, undershoot, and nuisance trips of the over-voltage protection, over-current protection or remote shutdown circuitry.

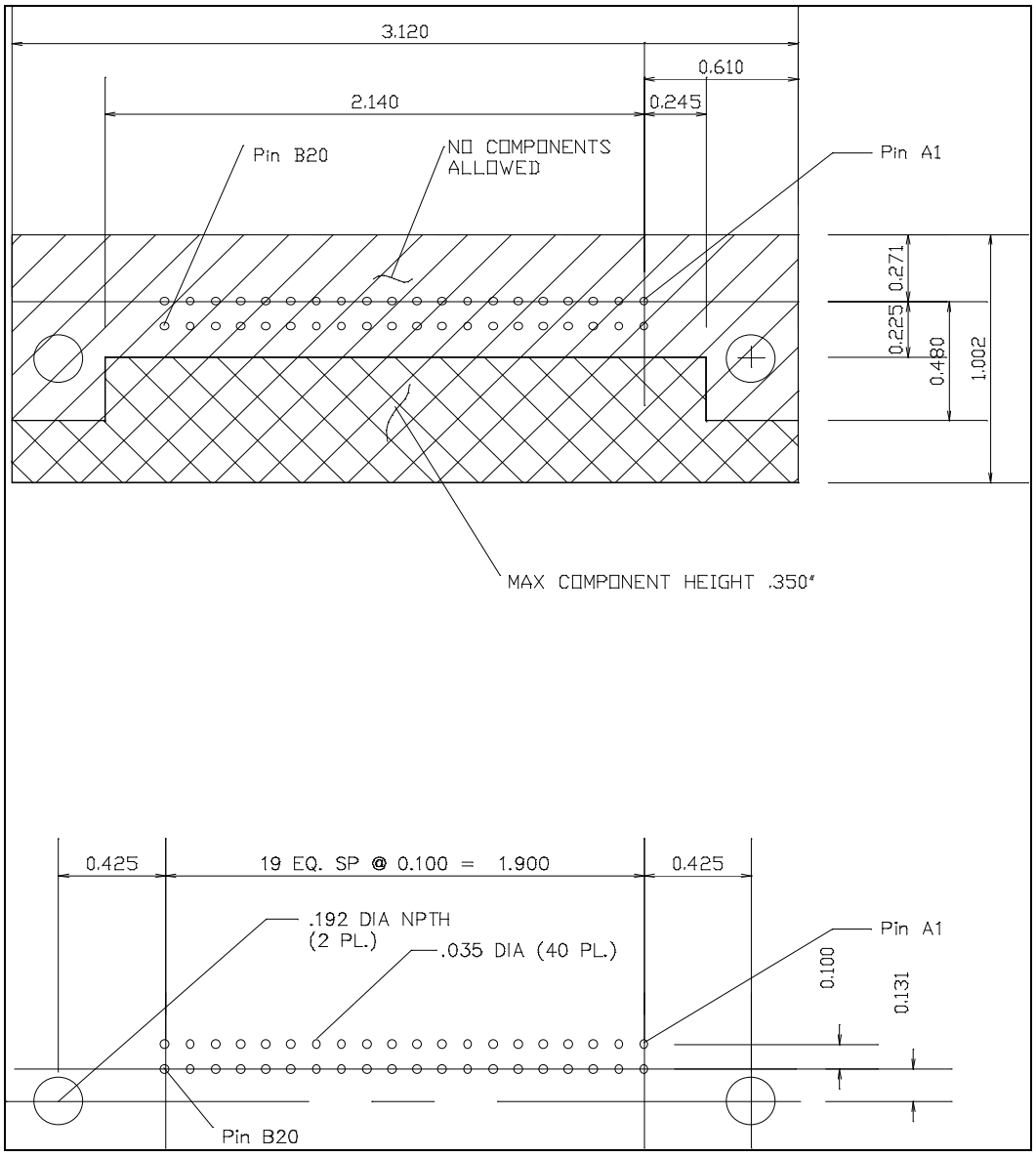

Figure 29. Alternative Mounting Configuration - Baseboard Pattern (Top View, Dimensions in Inches)

Shock and Vibration **GUIDELINE**

The DC-to-DC converter must not be damaged and the interconnect integrity not compromised during:

- A shock of 50G with an 11 millisecond half sine wave, non-operating, the shock to be applied in each of the orthogonal axes.
- Vibration of $0.01G^2$ per Hz at 5 Hz, sloping to $0.02G^2$ per Hz at 20 Hz and maintaining $0.02G^2$ per Hz from 20 Hz to 500 Hz, non-operating, applied in each of the orthogonal axes.

Electromagnetic **GUIDELINE**

Design, including materials, must be consistent with the manufacture of units that comply with the limits of FCC Class B and VDE 243 Level B for radiated emissions, given the existence of an external package around the converter with 20 dB of shielding.

Reliability **GUIDELINE**

The converter must be designed to function to electrical specifications, within the environmental specifications, with 60°C air at a velocity of 100 LFM directed along the connector axis.

10.3.1. Component De-rating **GUIDELINE**

The following component de-rating guidelines must be followed:

- Semiconductor junction temperatures must be < 115°C with ambient at 50°C.
- Capacitor case temperature must not exceed 80% of rated temperature.
- Resistor wattage de-rating must be > 50%.
- Component voltage and current de-rating must be > 20%, the effects of ripple current heating must be accounted for in this de-rating.

10.3.2. Mean Time Between Failures (MTBF) **GUIDELINE**

Design, including materials, must be consistent with the manufacture of units with an MTBF of 500,000 hours of continuous operation at 55°C, maximum-outputs load, and worst-case line, while meeting specified requirements. MTBF must be calculated in accordance with MIL-STD-217F.

Safety **GUIDELINE**

Design, including materials, must be consistent with the manufacture of units that meet the standards of UL flammability specifications per 94V-0.

11.0 Pentium® Pro Processor Power Distribution Network Modeling

The following power model is provided in HSPICE format to allow simulation of the power distribution sub-system. This is the same model used by Intel for simulation of early power supply solutions. It is a Norton equivalent circuit created to estimate a worst case di/dt of about 1.0A/ns with a peak current of 10 Amps and a minimum current of 0A. This model is for a 150MHz clock and includes the switching transients that can occur during full power operation, as well as the initial current ramp from low to high current states. A similar effect occurs when entering stop clock from full power. This can also be modeled by changing this model symetrically.

This information should be used solely as a baseline for system development and should be followed by actual measurements of the power islands as explained in Section 8.

11.1. Using the Power Distribution Model

This model assumes a peak current of 10 Amps and a minimum current of 0 Amps. This is only a slightly wider swing than the specification for the 150MHz Pentium Pro processor. To design for a flexible motherboard, one should scale this model upwards. Note that a change in frequency will affect this model somewhat, but not drastically.

This model includes a socket that meets the guideline of 4.5nH mated inductance per pin. DO NOT ADD A SOCKET INTO YOUR MODEL as this is already comprehended in the Pentium Pro processor power model.

The model presented here has been shown to correlate with the Intel's internal models within the range of normal operation. However, as the voltage at the Pentium Pro processor pins departs from the ±5% voltage

specification, the accuracy will suffer. Specifically, the Pentium Pro processor die will consume more current at high voltage and less current at low voltage while the SPICE model does not exhibit this behavior. Therefore, bear in mind that while this model can be used to accurately model a system that meets or exceeds the ±5% voltage requirement, it cannot be used to accurately describe how far out of specification a poorly designed system lies.

11.2. Power Distribution Model

This is the HSPICE format power distribution model for a socketed Pentium Pro processor. The schematic is shown in Figure 30. Note that the last line of the model includes "R 73.9NS". This commands the simulator to continuously repeat the last portion of the waveform from time 73.9nS until the end of the simulation.

```
Ri 100 101 0.01
Li 101 102 121pH
Ci 102 103 160nF

IPULSE 100 103 PWL(0 0 4.1NS 0 18.8NS 14.78
+ 20NS 13.78 22NS 13.48 27.3NS 10.31
+ 31.8NS 7.874 + 35NS 10.668 39.5NS 8.17
+ 42.9NS 8.91 45.5NS 8.574 47.1NS 7.514
+ 50.1NS 8.633 56.  4NS 11.08 + 58.5NS 10.77
+ 61.8NS 13.71 67.5NS 9.17 + 72.3NS 7.26
+ 73.9NS 5.91 77.8NS 7.20 83.4NS 11.11
+ 85.4NS 11.26 88.6NS 14.54 95.9 NS 9.11
+ 100.8NS 5.576 R 73.9NS)
```

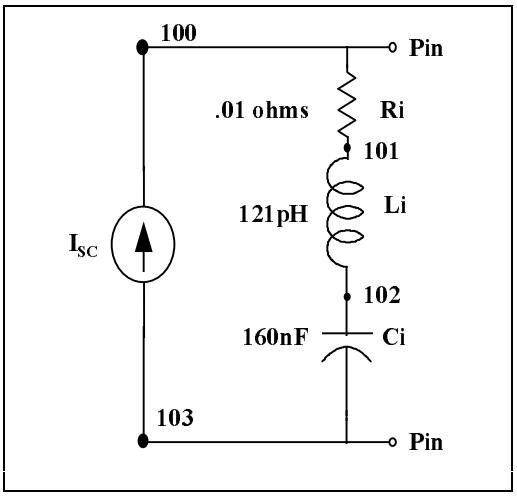

Figure 30. Socketed Pentium® Pro Processor Power Distribution Model Schematic

Figure 31 shows the short-circuit current used in the HSPICE model plotted vs. time.

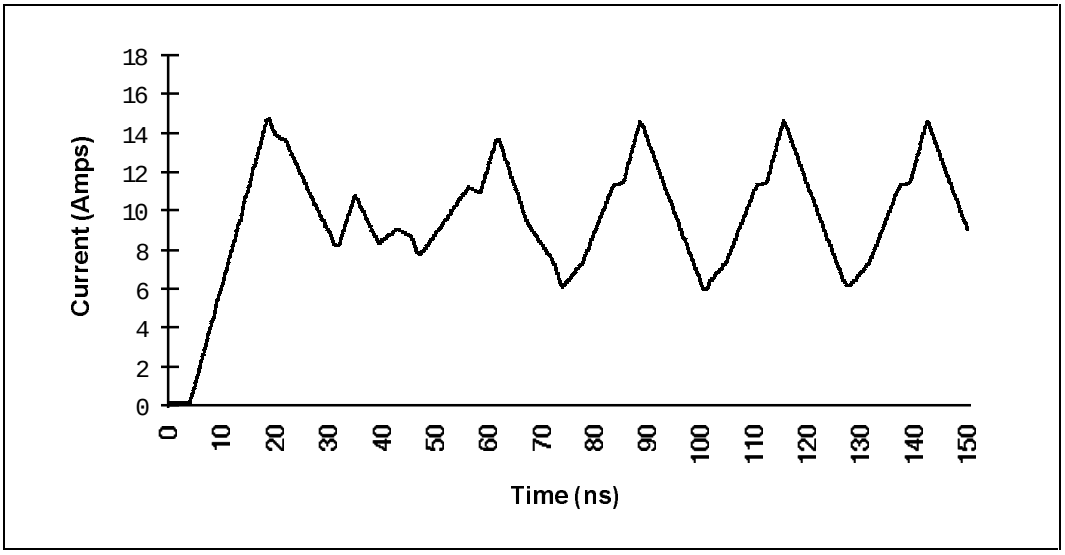

Figure 31. Power Distribution Model Short-Circuit Current